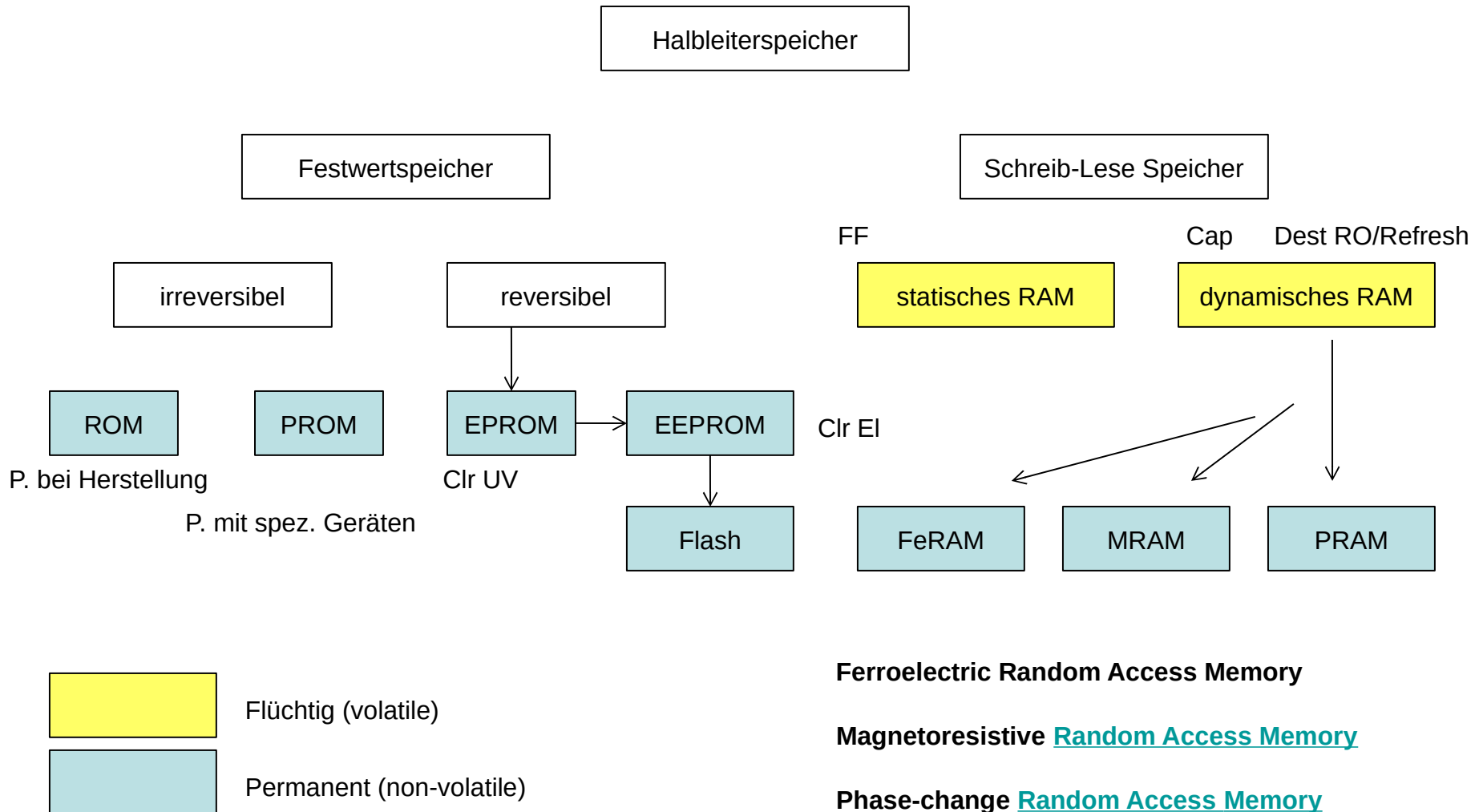


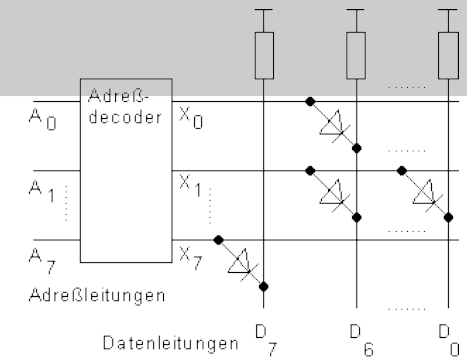
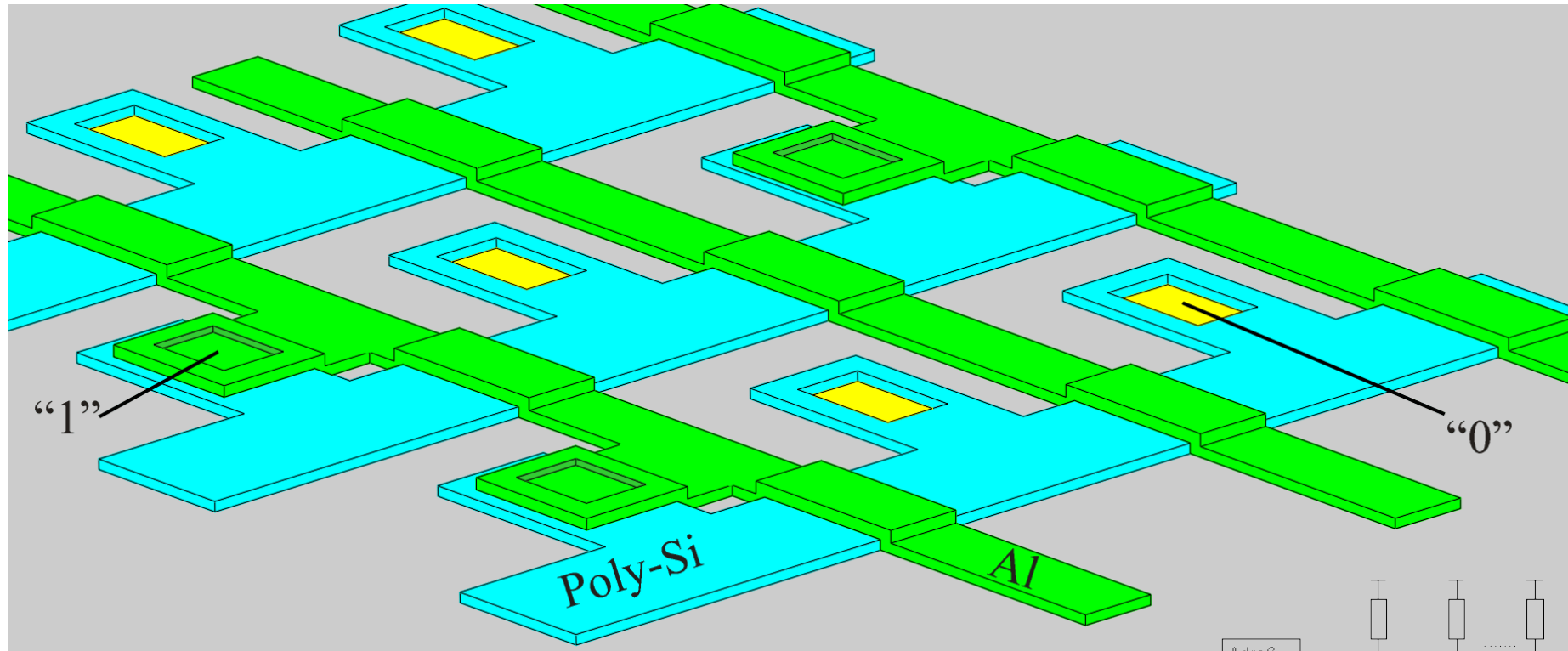
Design digitaler Schaltkreise

Klassifizierung



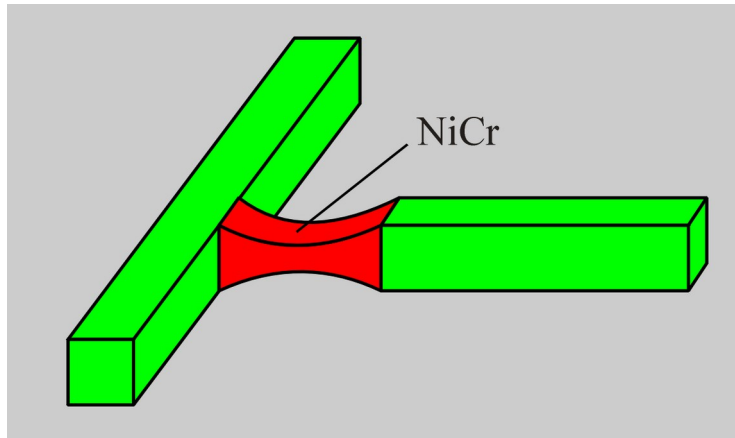
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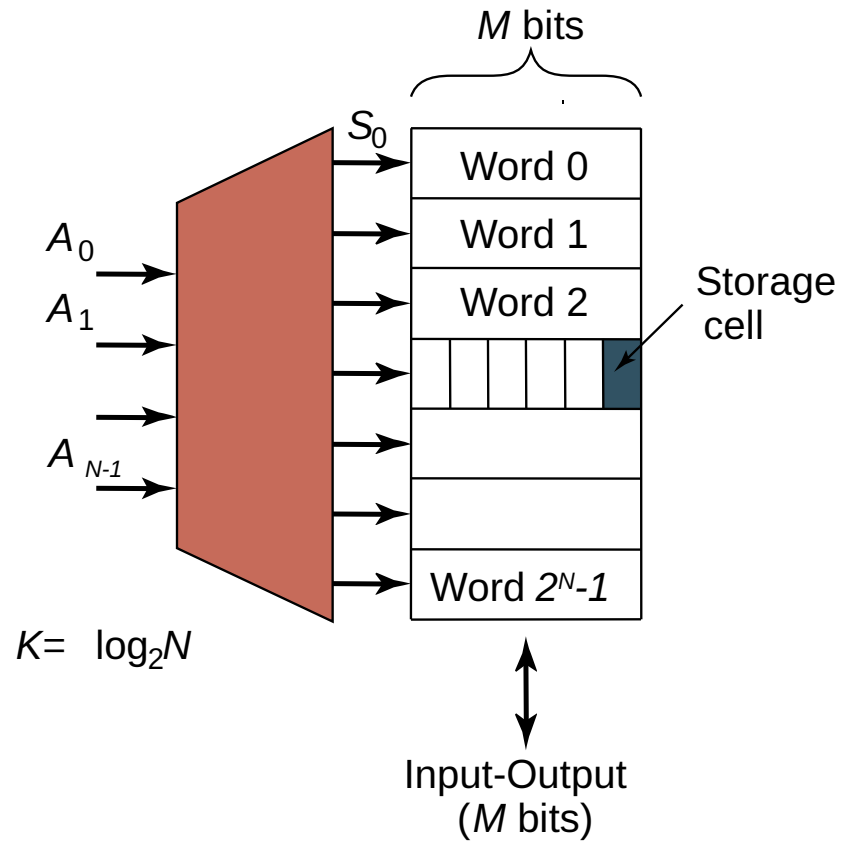
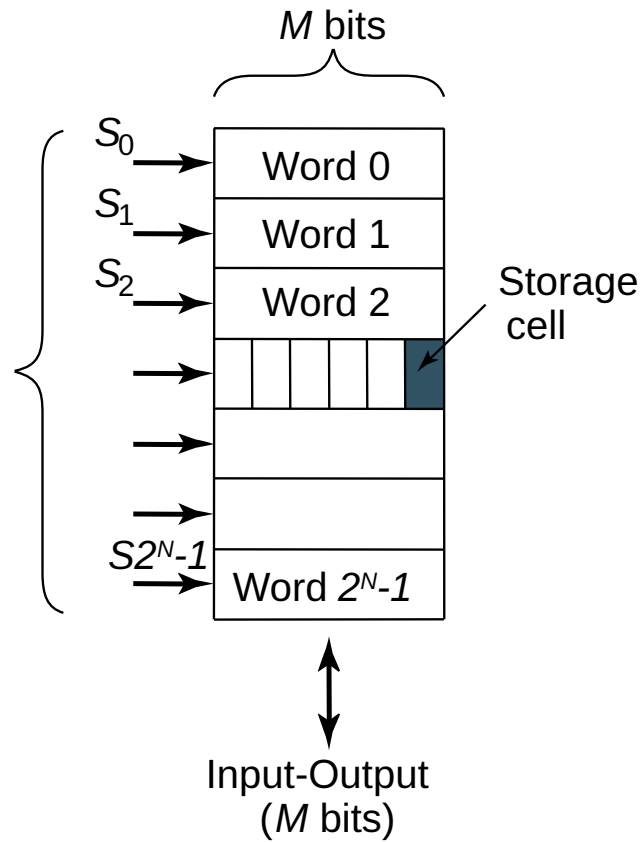
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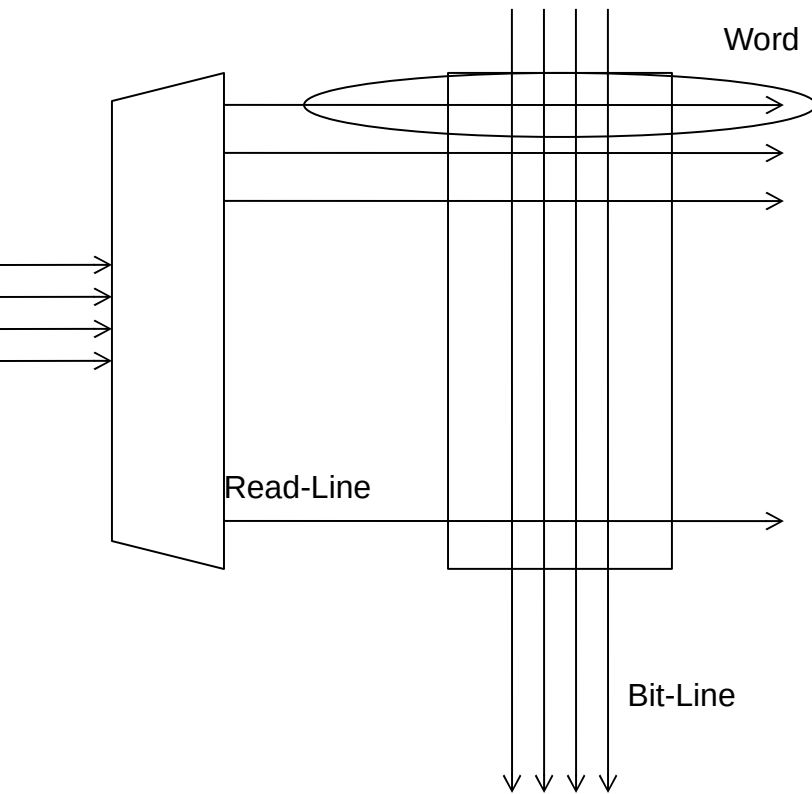


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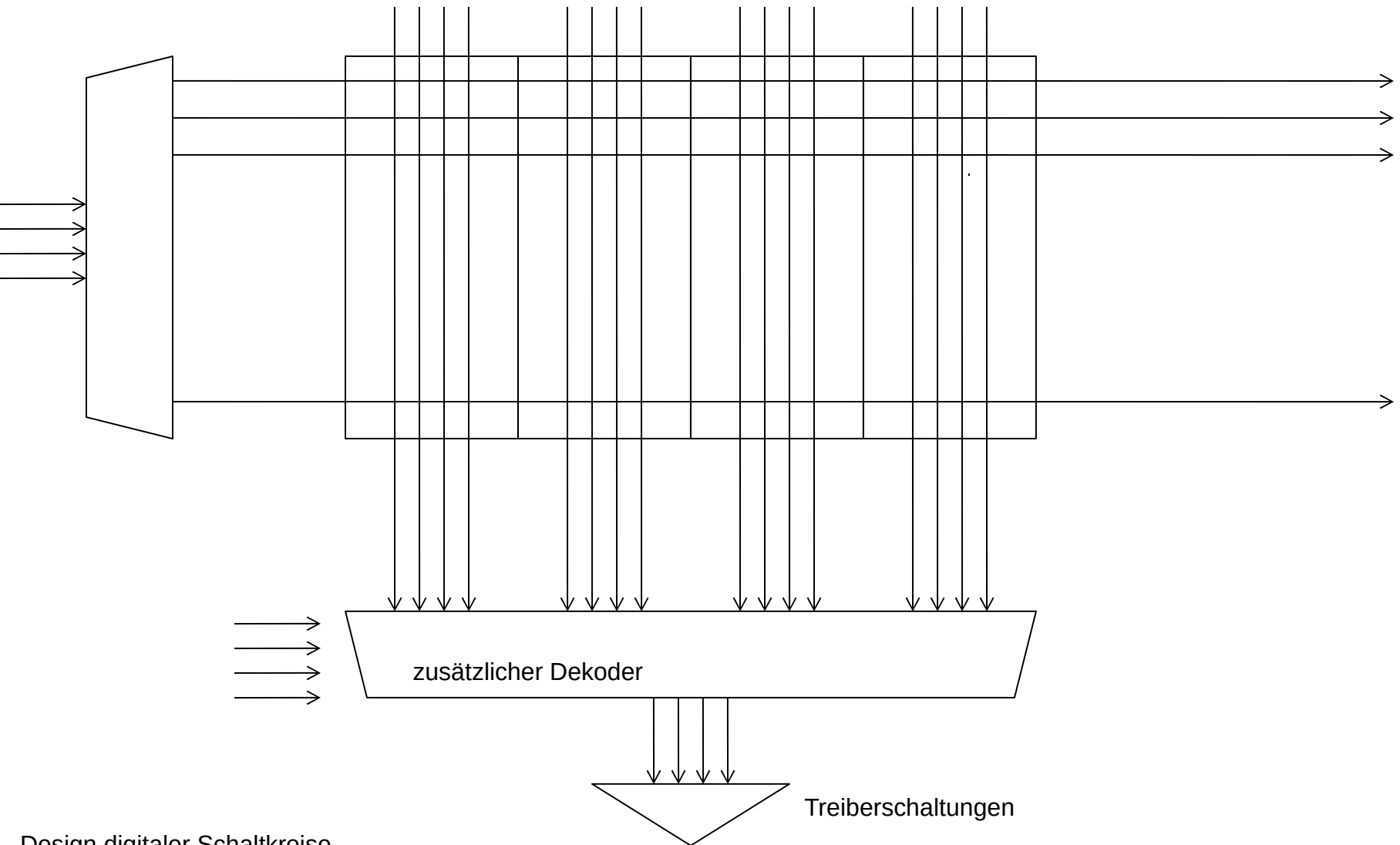
PROM





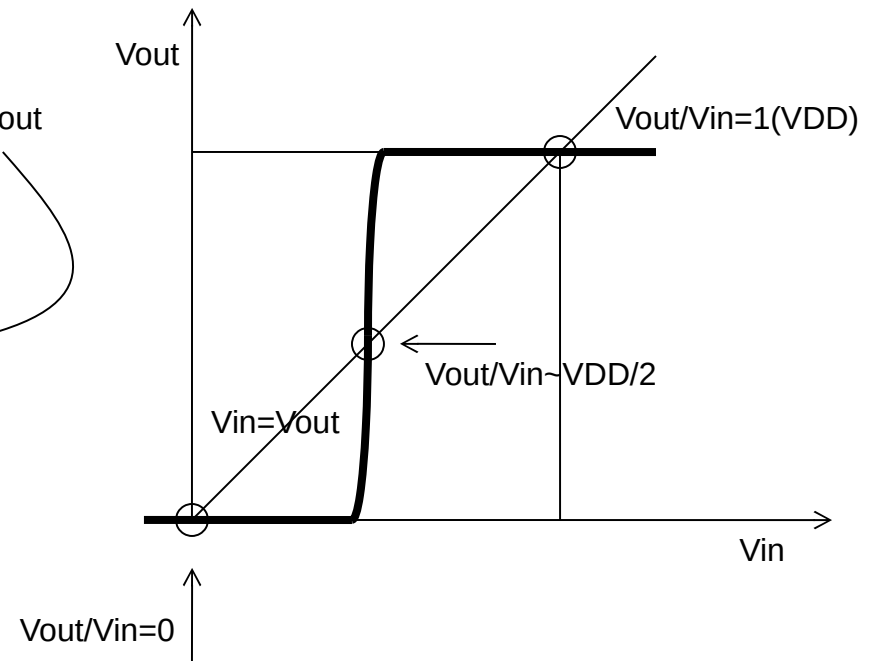
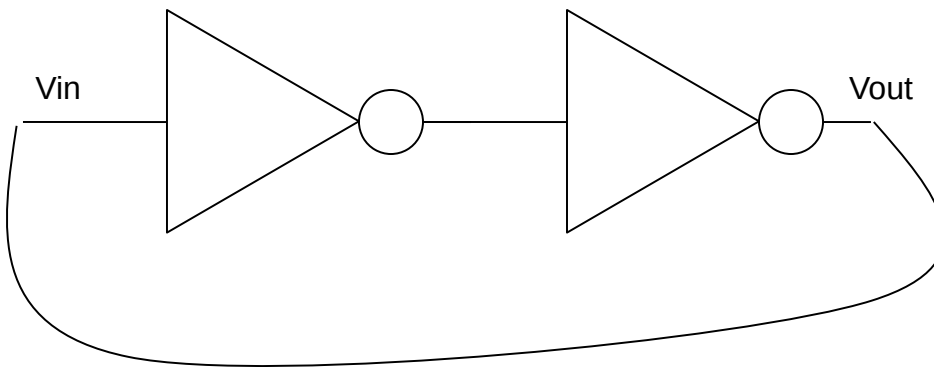


Aspect ratio!

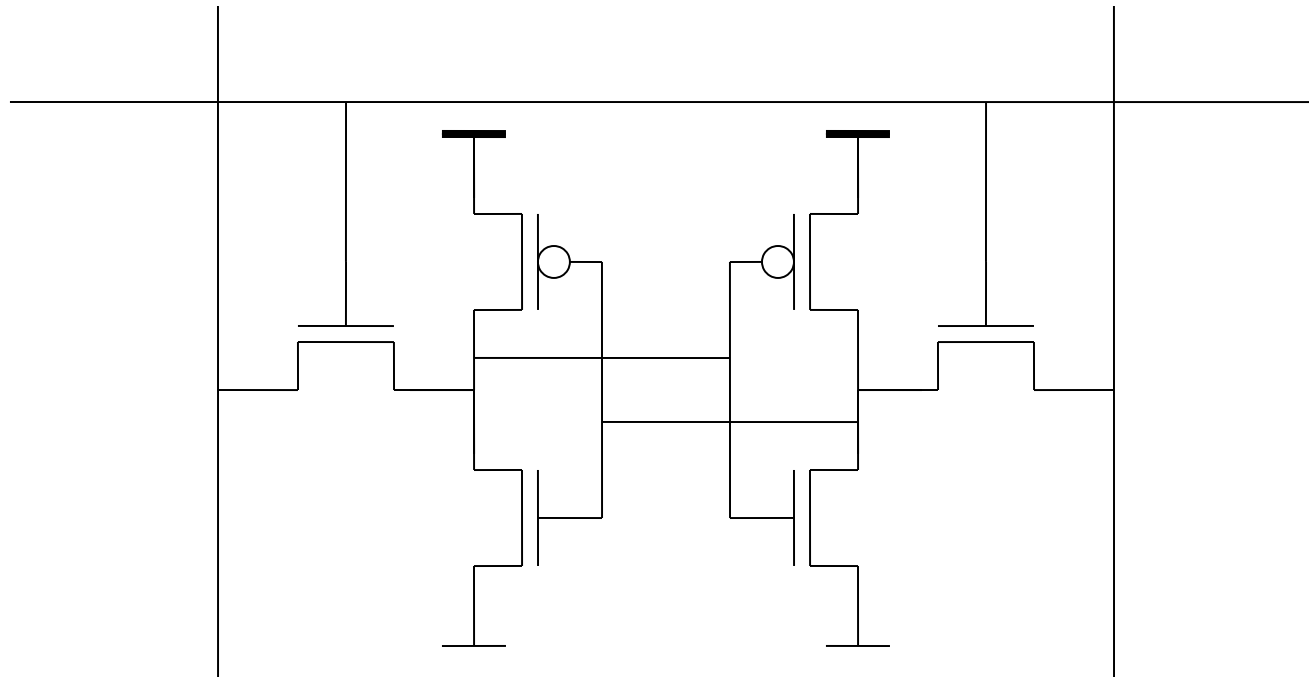


SRAM

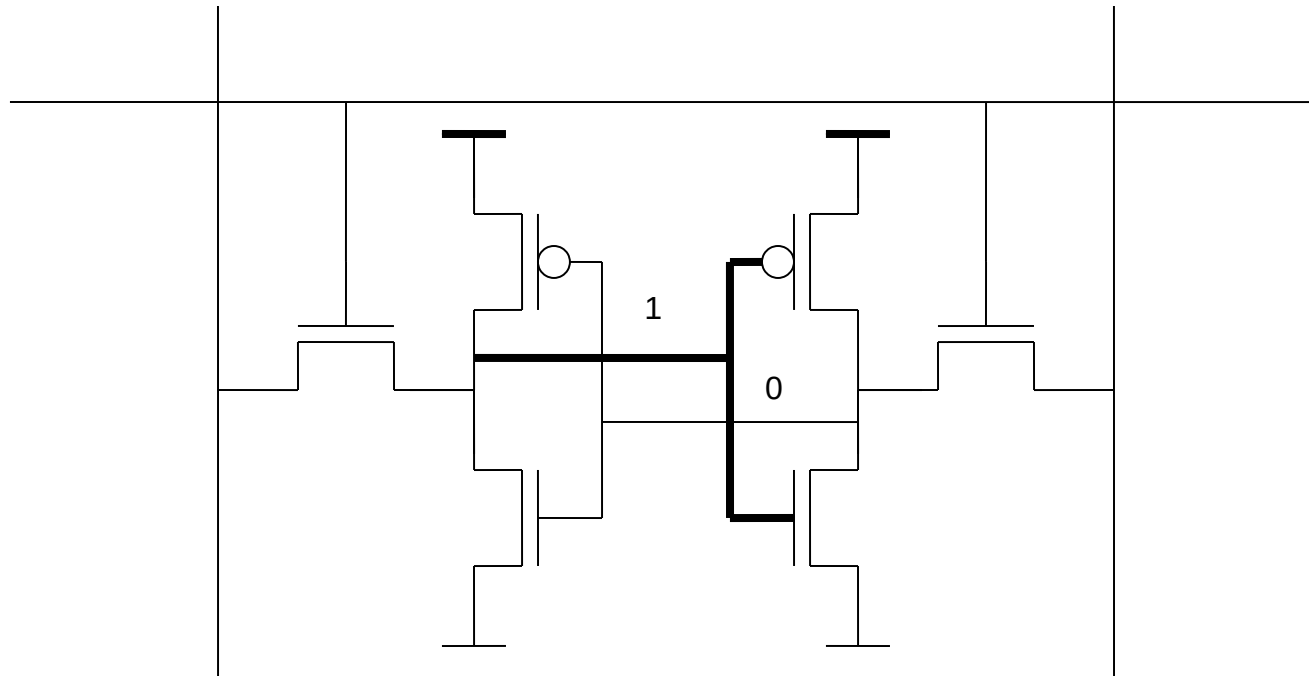
- Statische Speicherzellen
- Wenn wir den Ausgang des zweiten Inverters mit dem Eingang des ersten verbinden, haben wir $V_{in} = V_{out}$.
- Der Zustand der Schaltung liegt im Schnittpunkt der Kennlinie $V_{out} = f(V_{in})$ und der Geraden $V_{out} = V_{in}$.



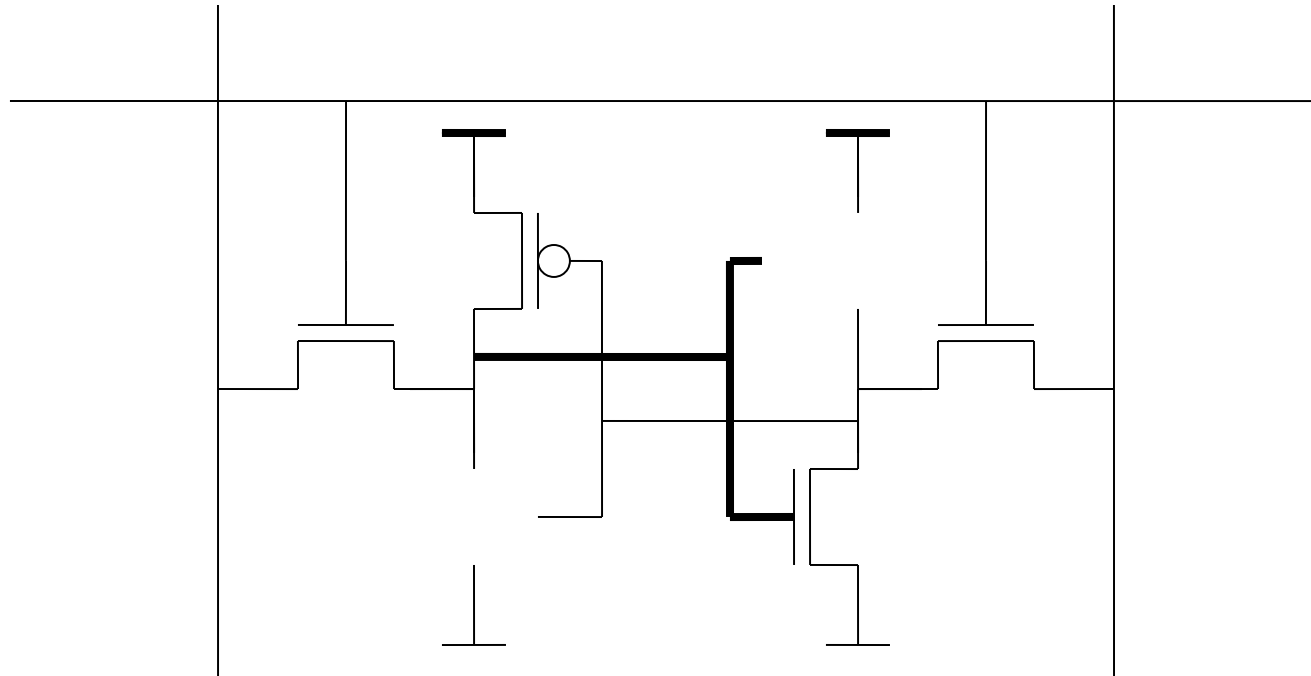
- SRAM



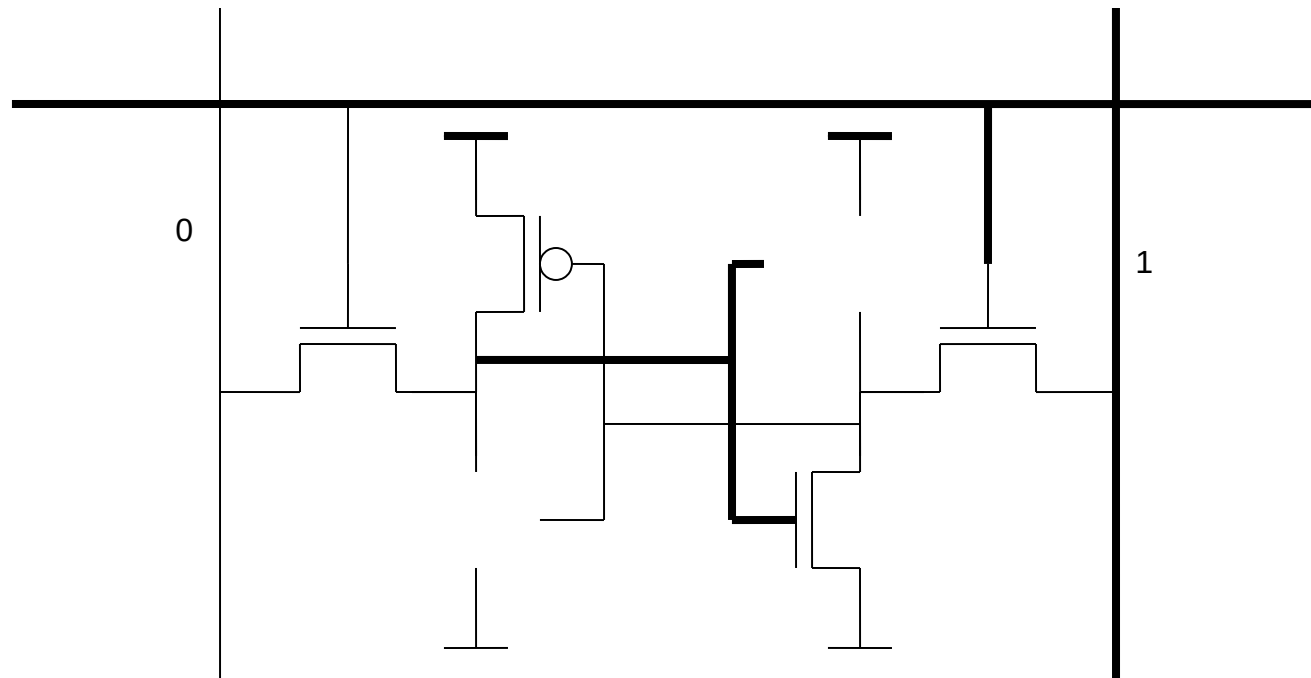
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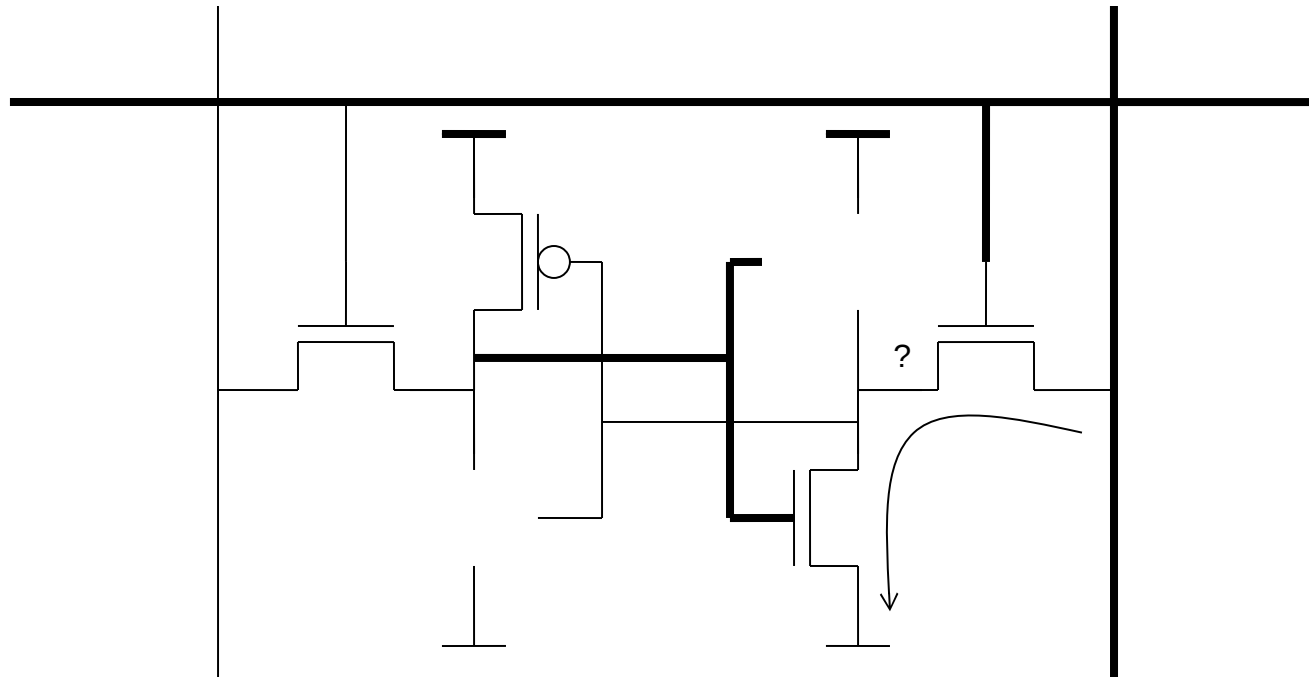
- SRAM



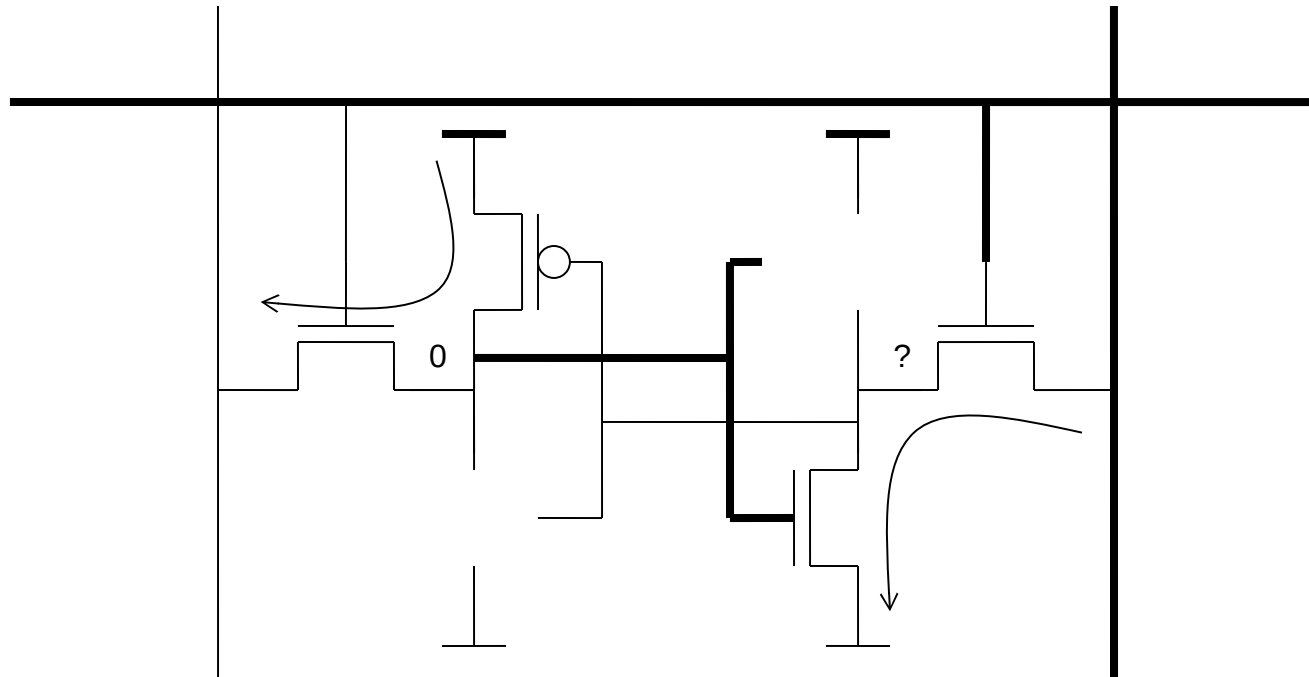
- SRAM



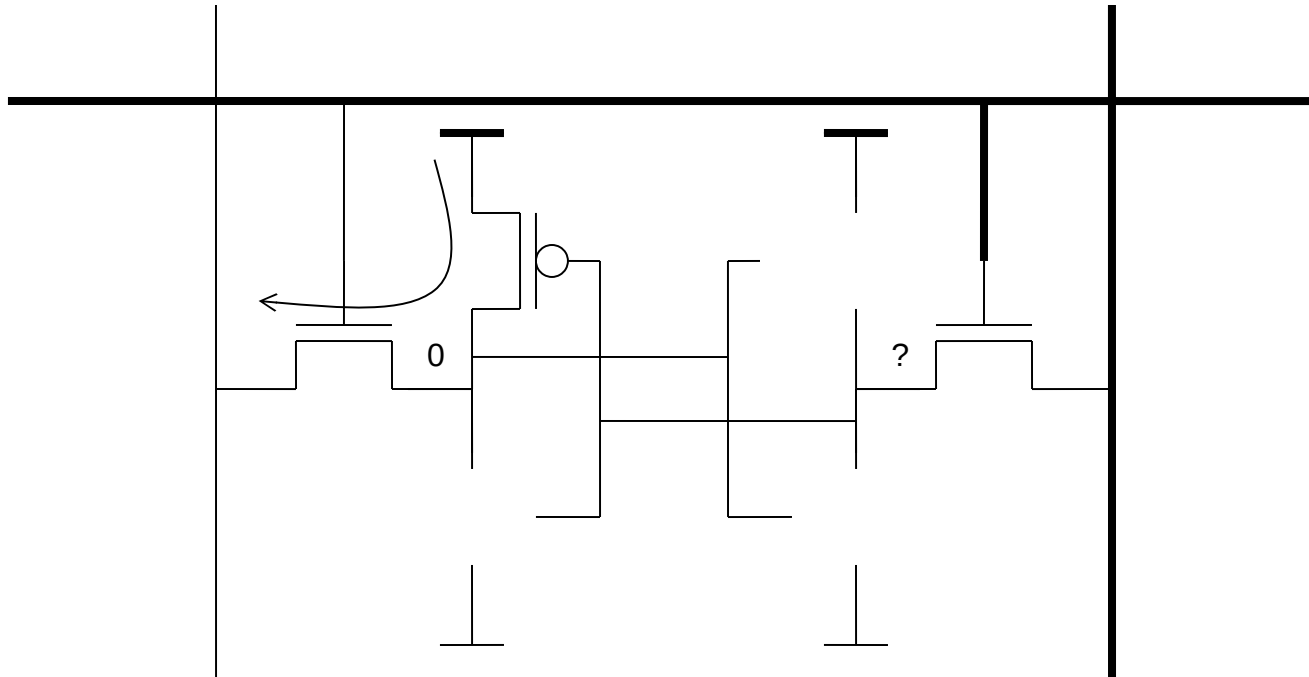
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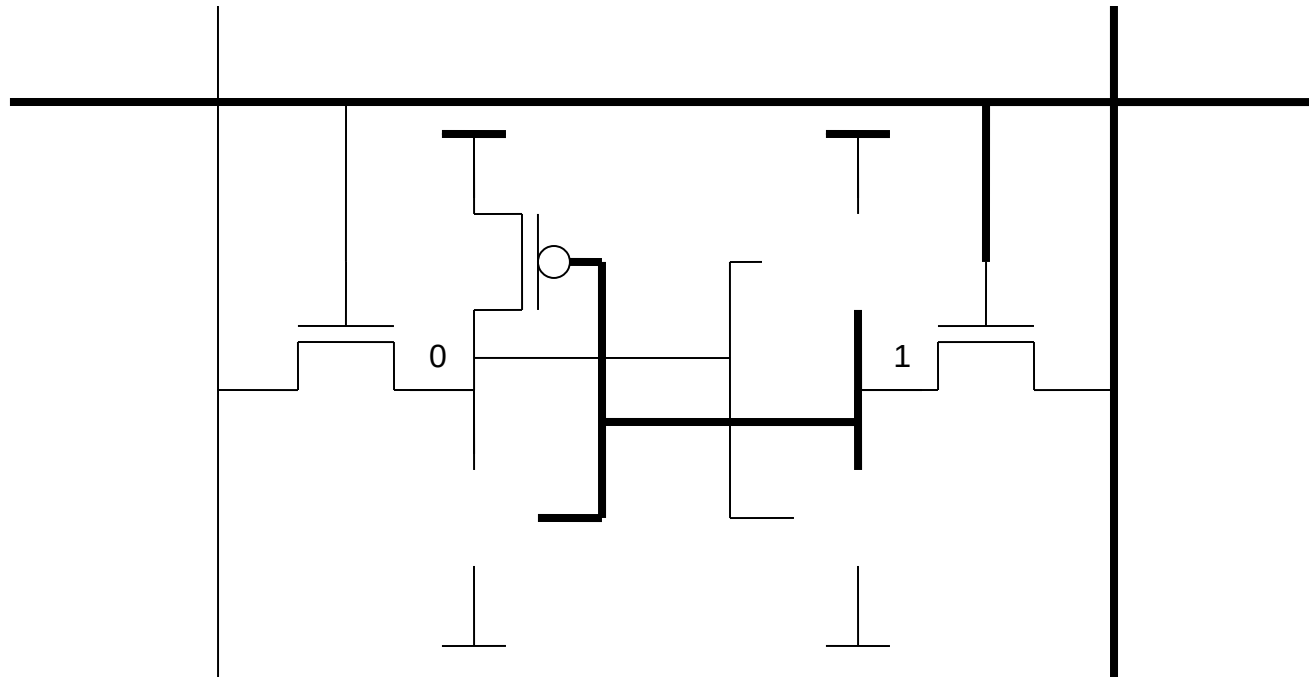
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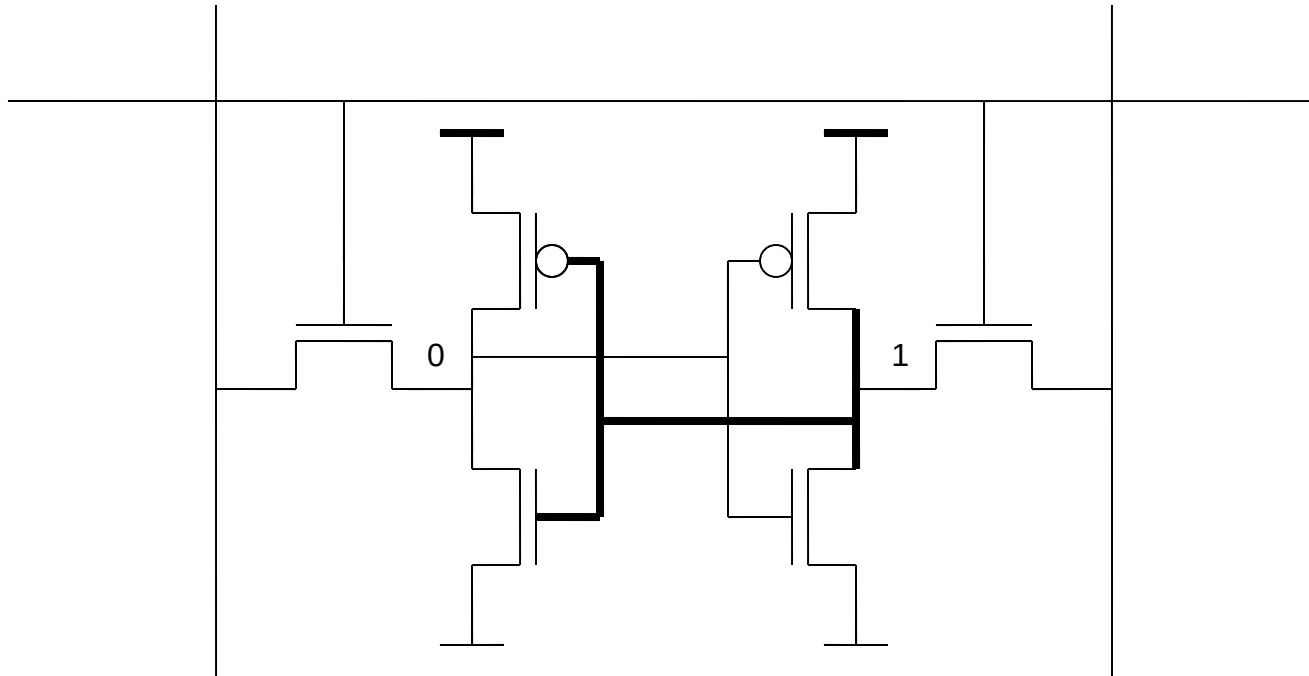
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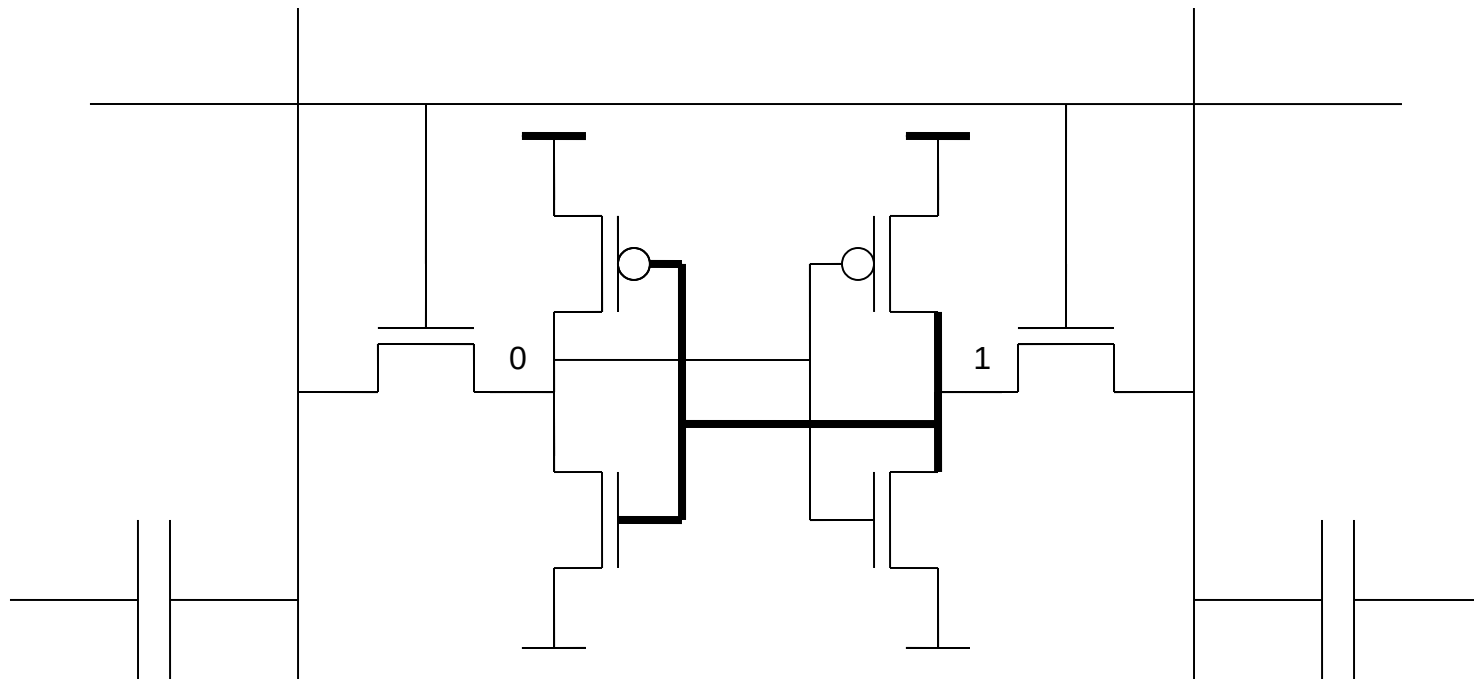
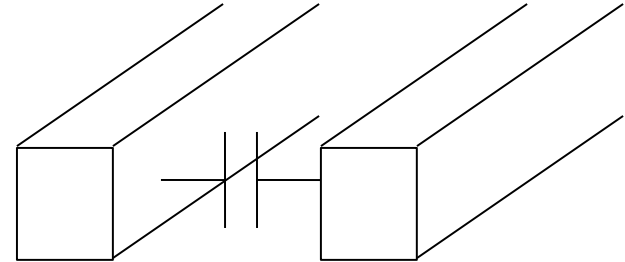
- SRAM



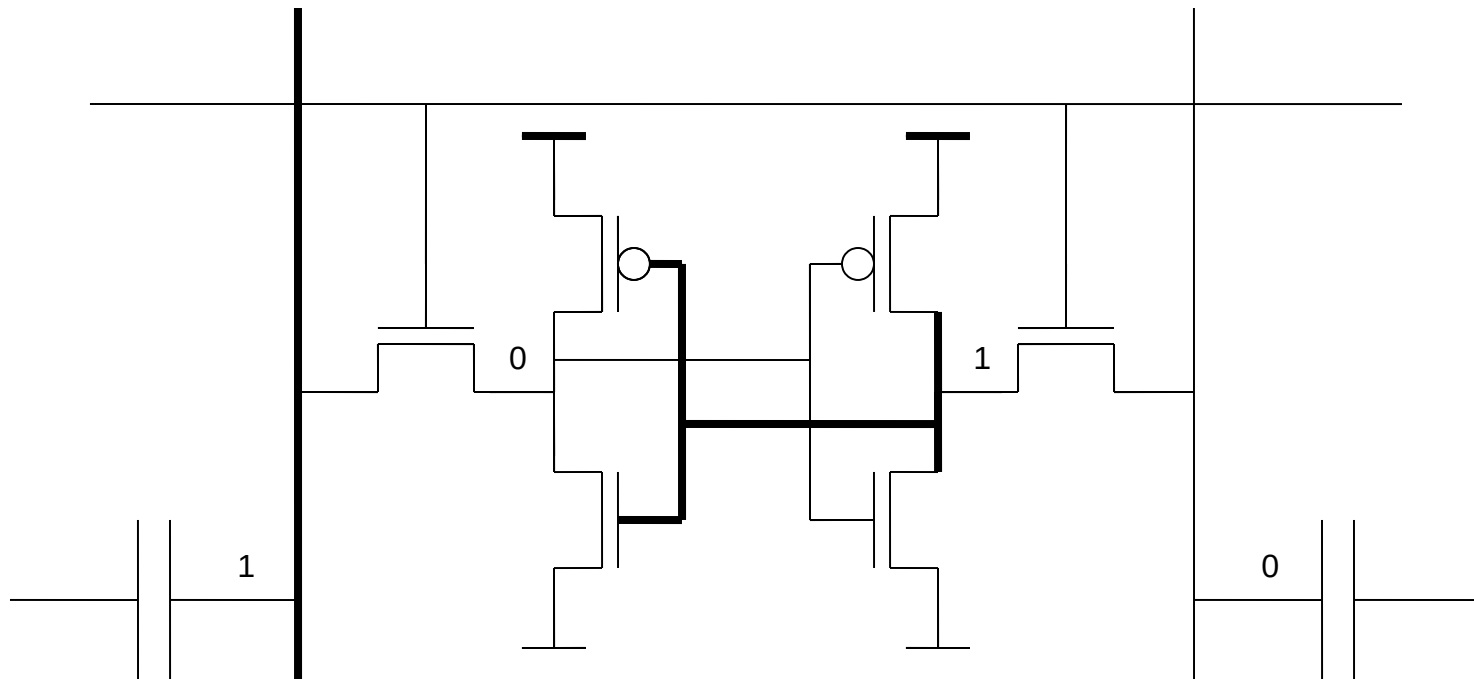
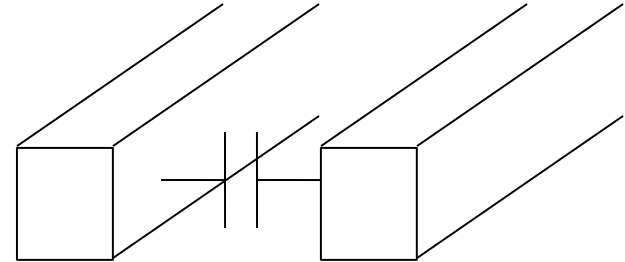
- SRAM



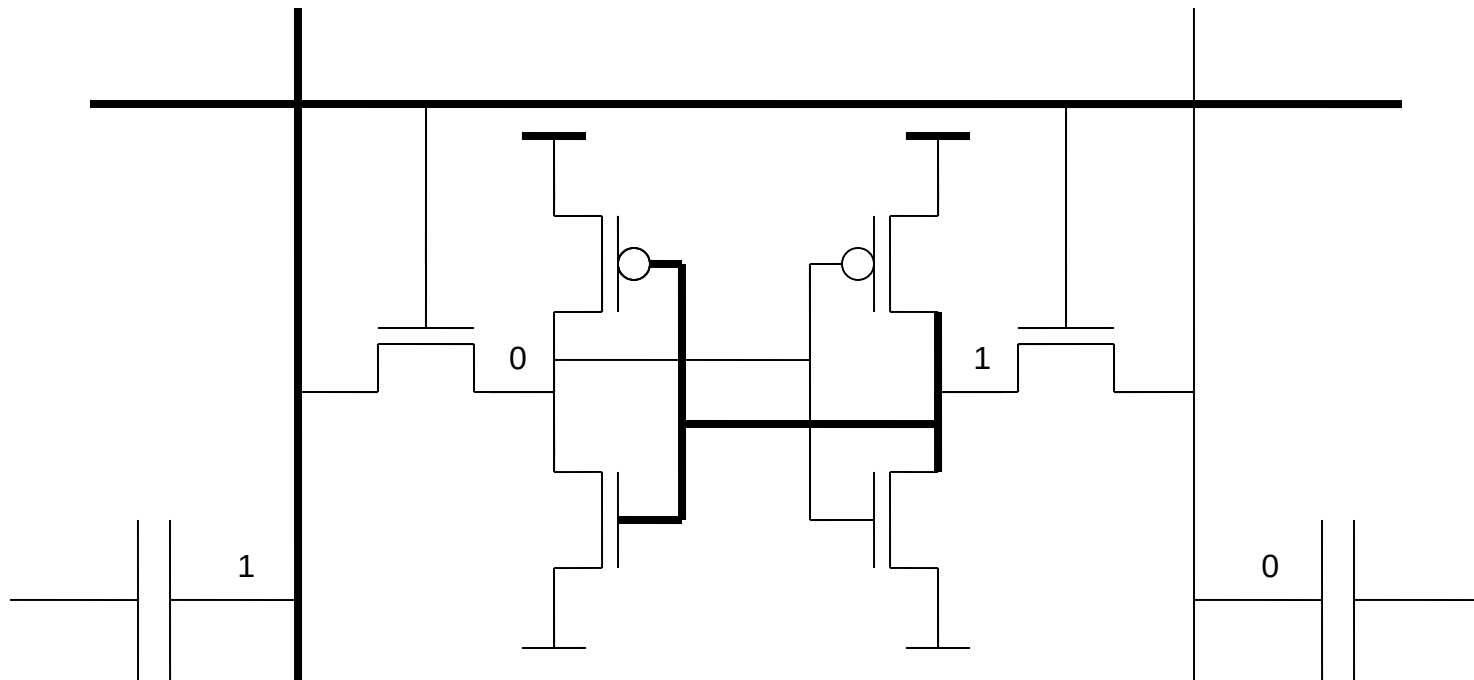
- SRAM



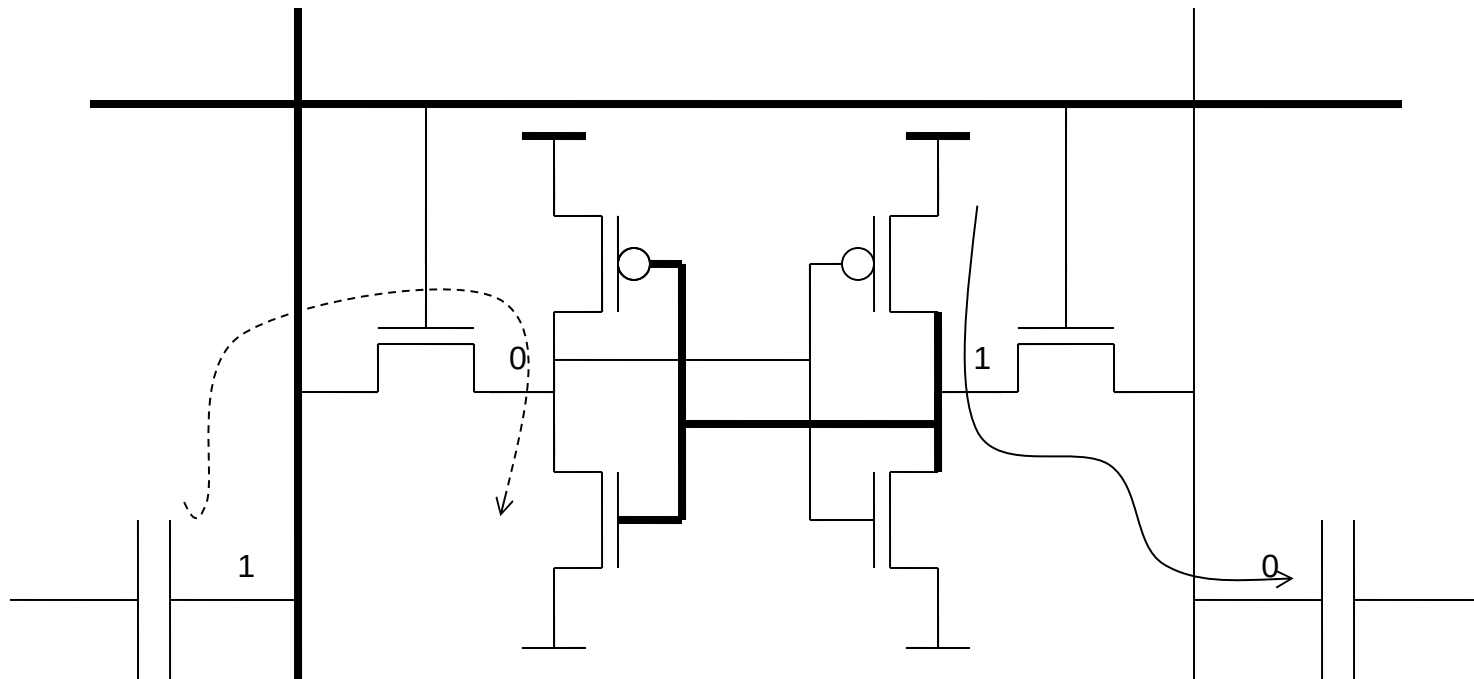
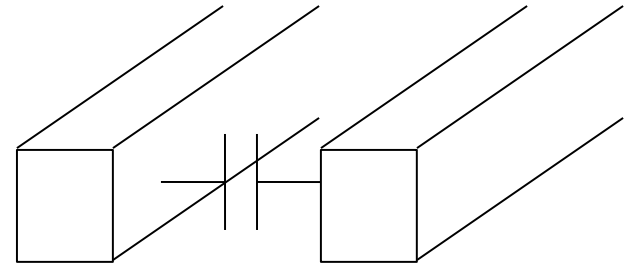
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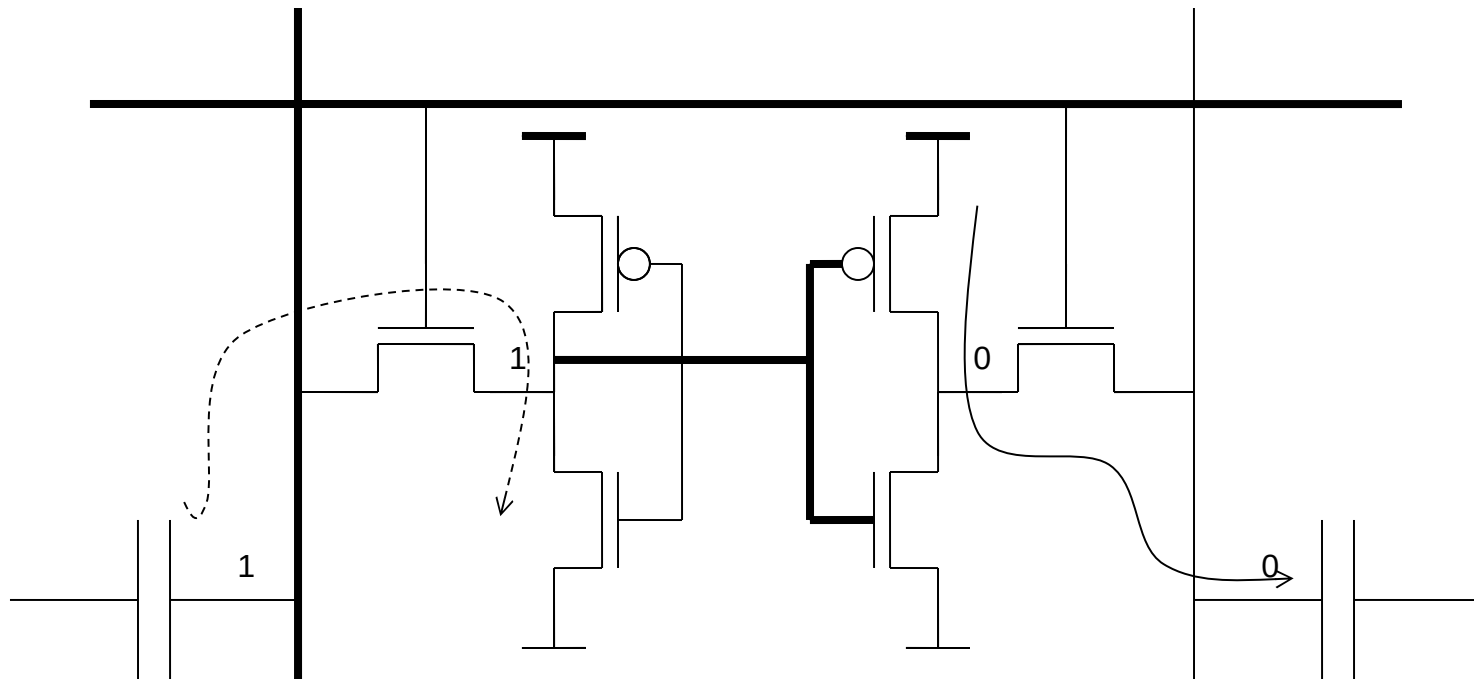
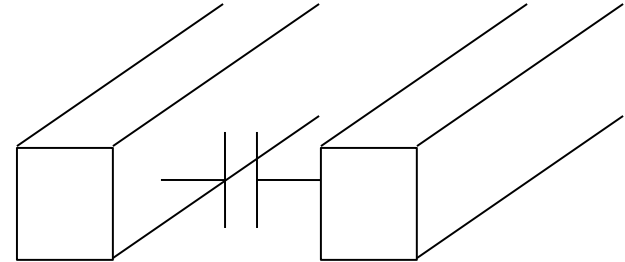
-
- A diagram showing two rectangular blocks, one on the left and one on the right, connected by a horizontal line. A vertical line intersects the horizontal line between the two blocks.



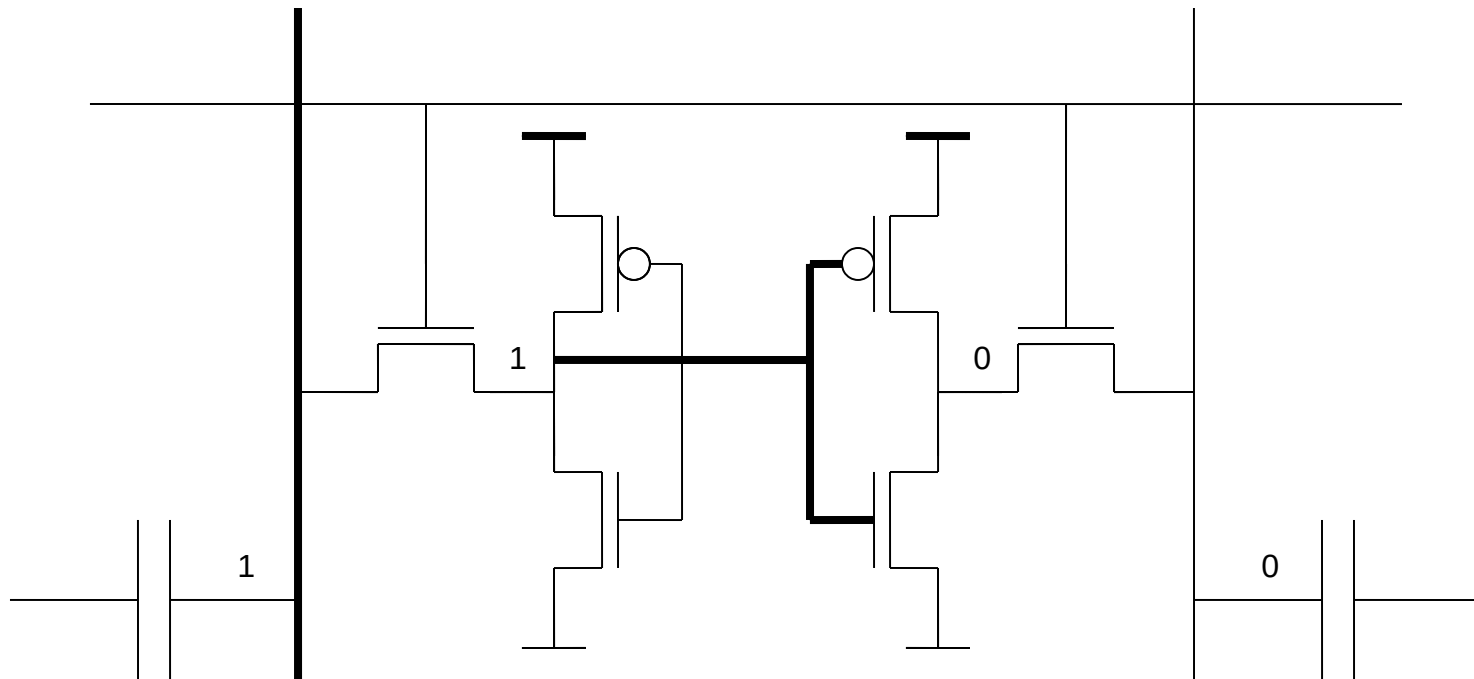
- SRAM



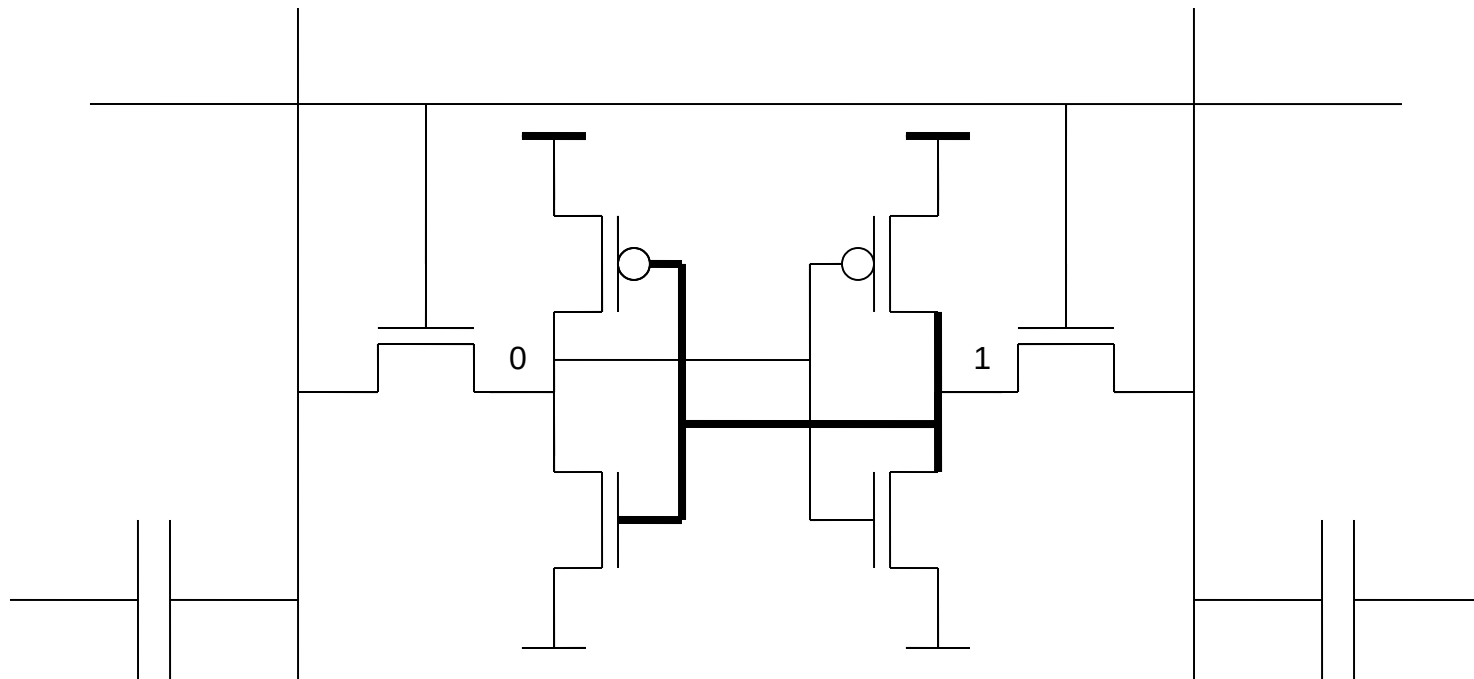
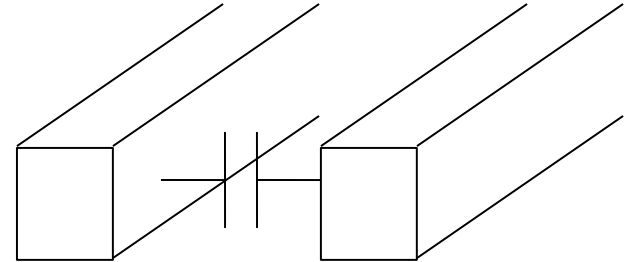
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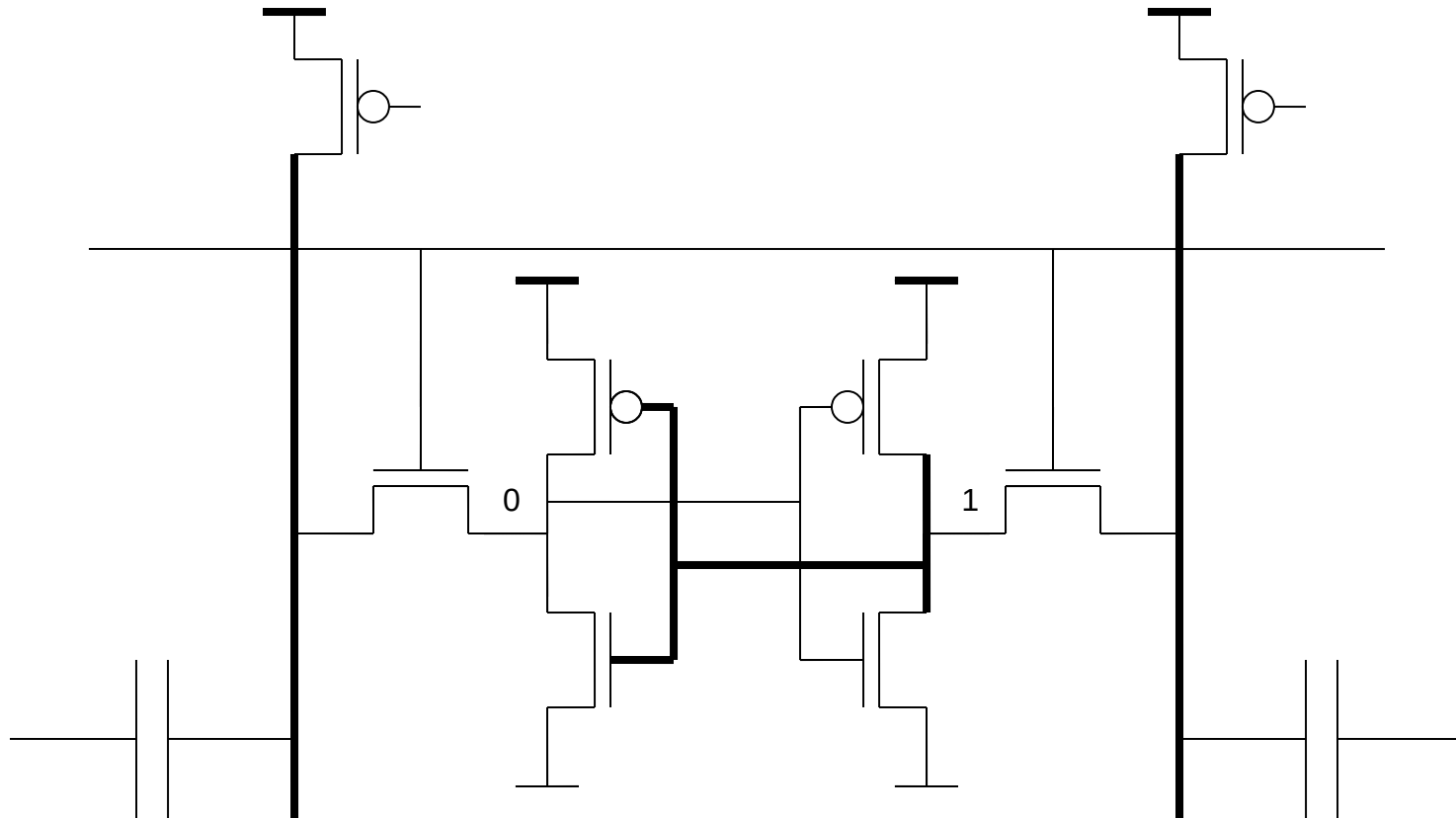
-
- A diagram showing two rectangular blocks, one on the left and one on the right, connected by a horizontal line. A vertical line intersects the horizontal line between the two blocks.



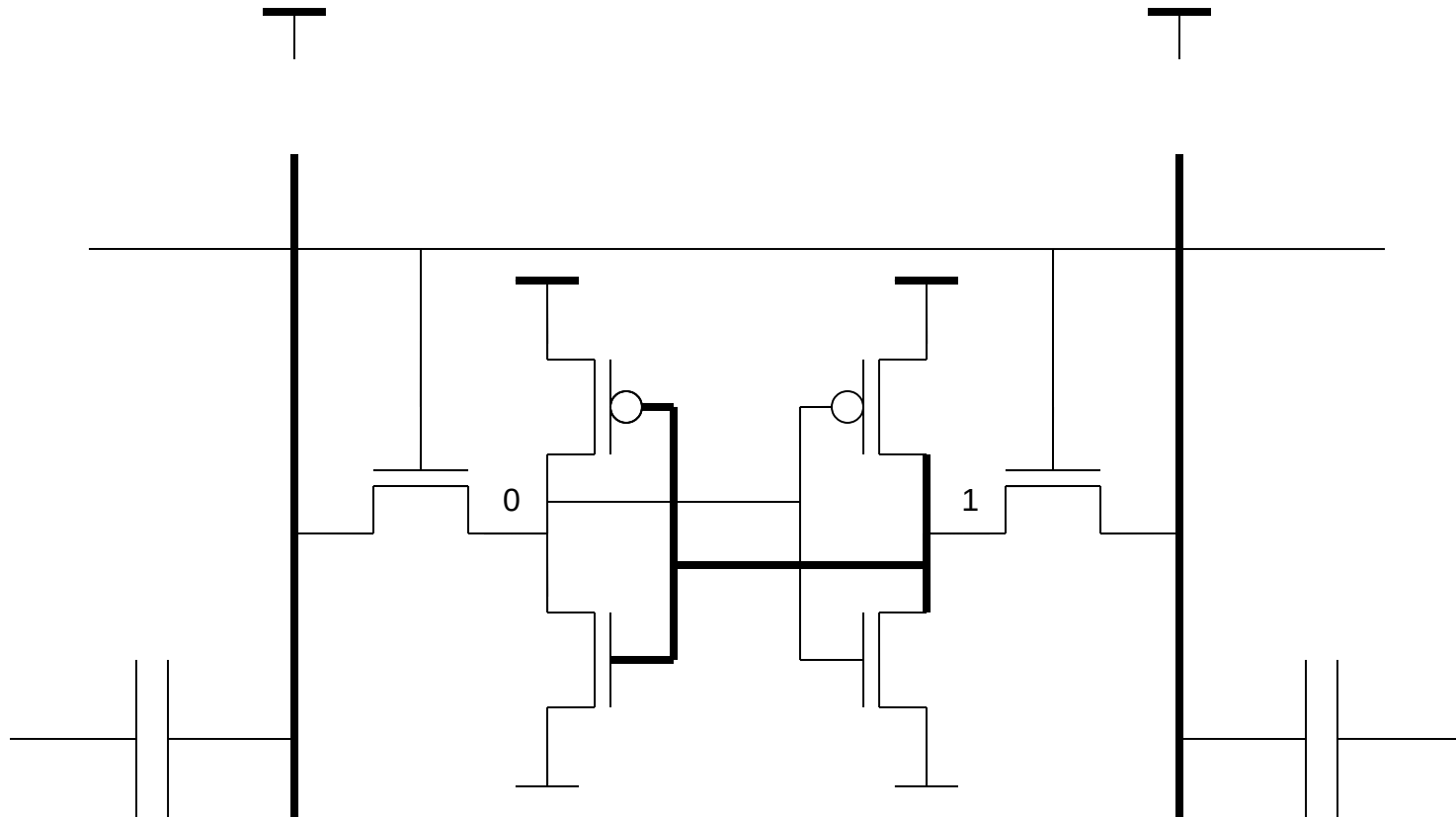
- SRAM



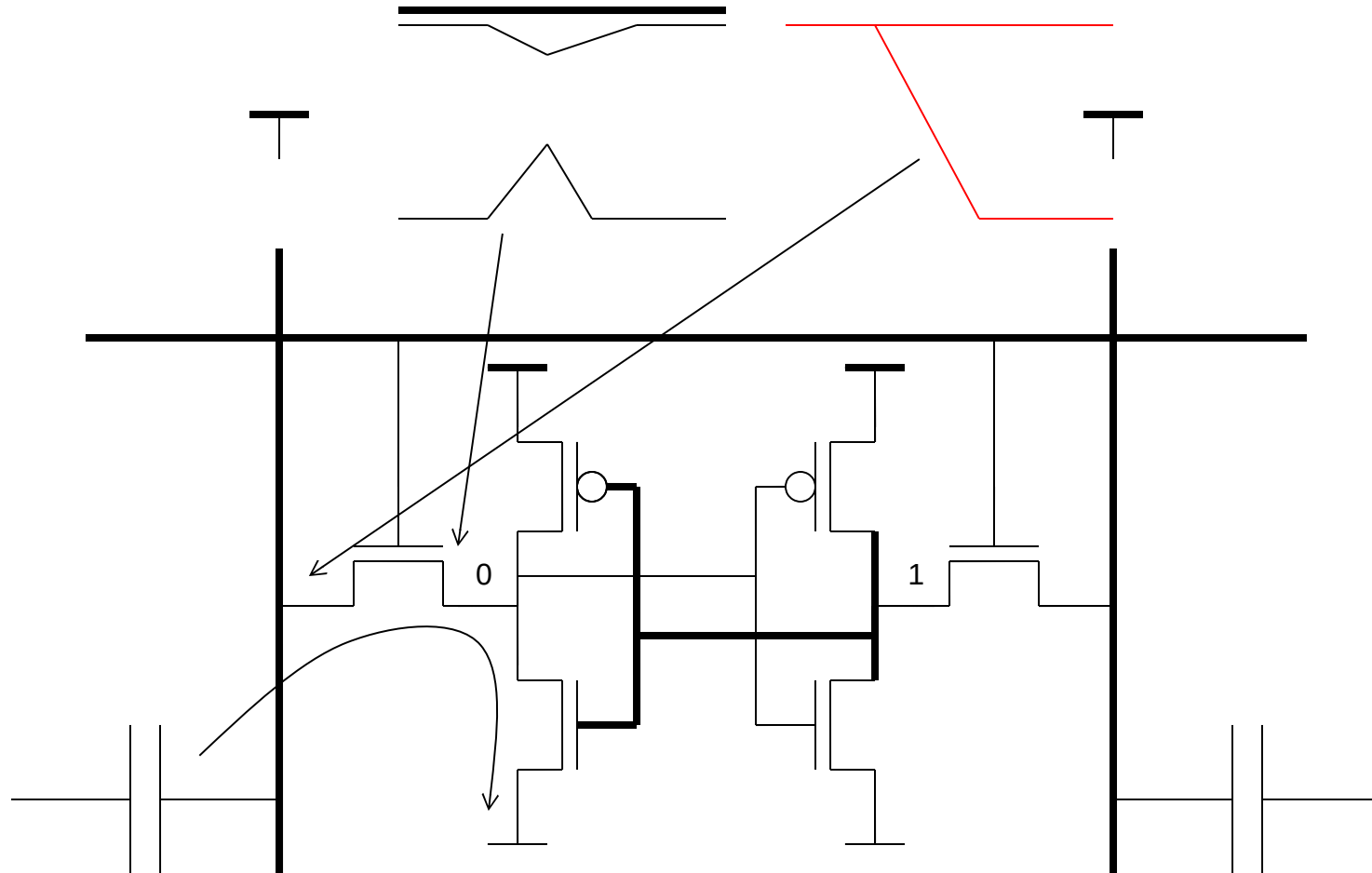
- SRAM



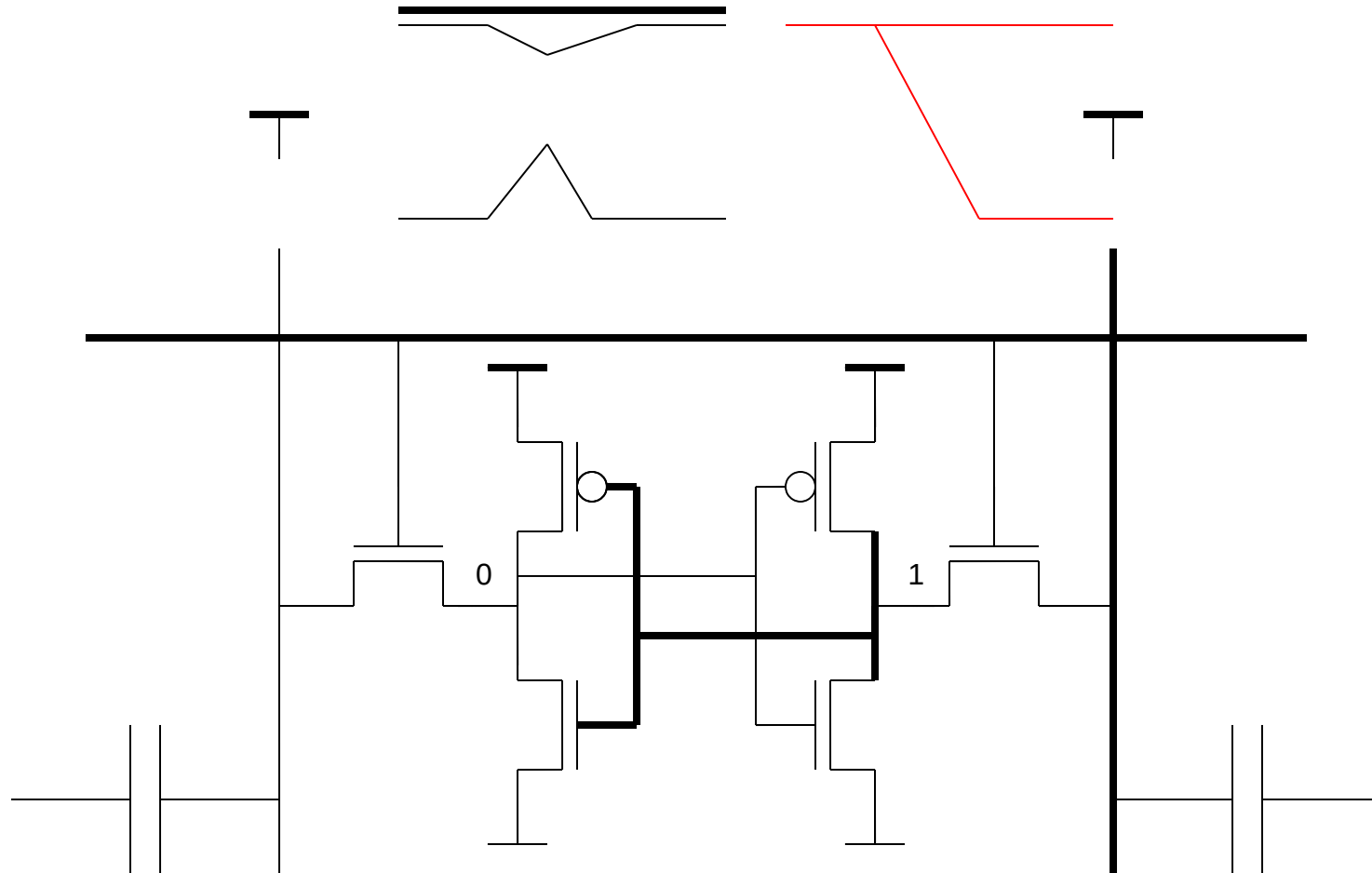
- SRAM



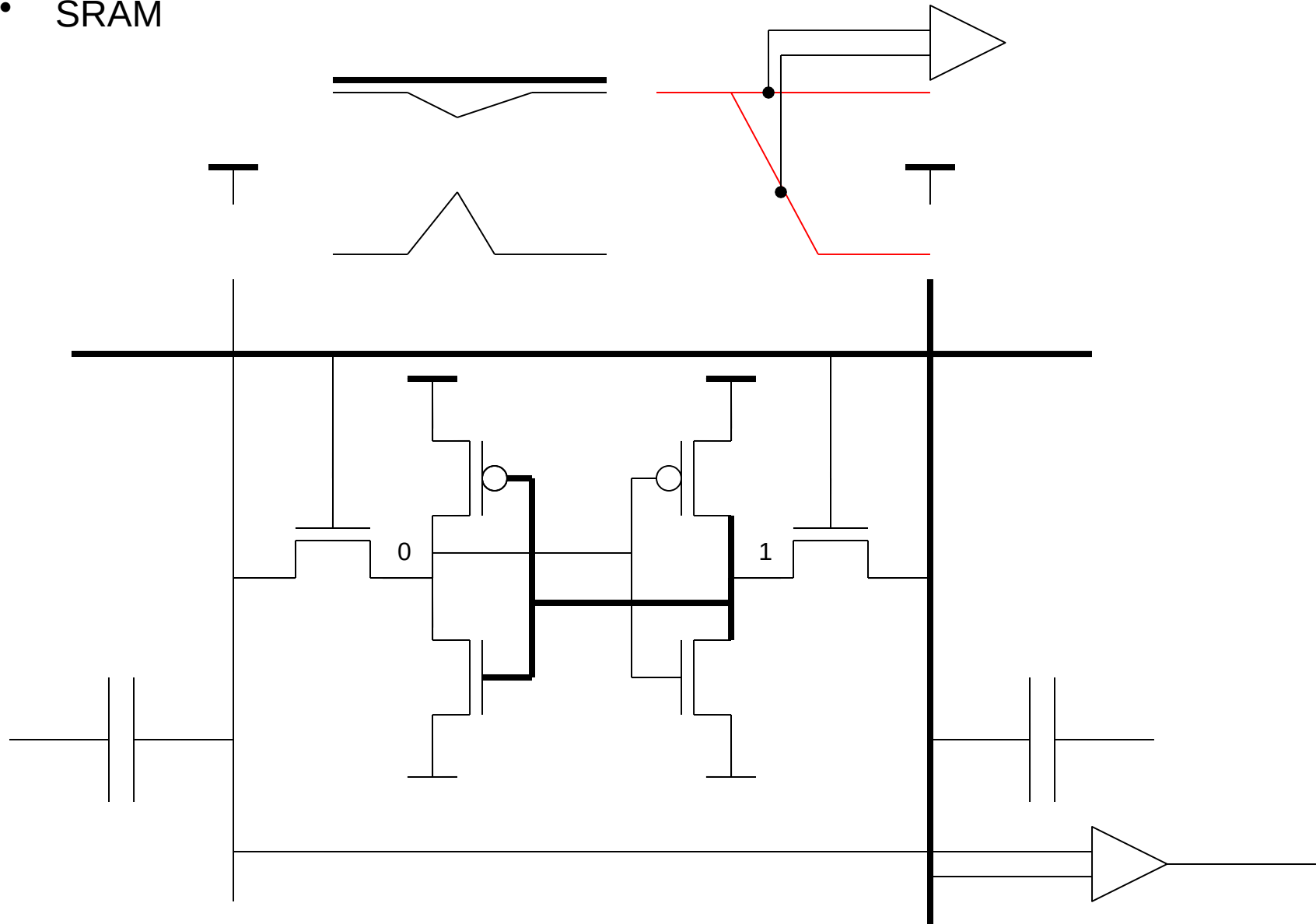
- SRAM



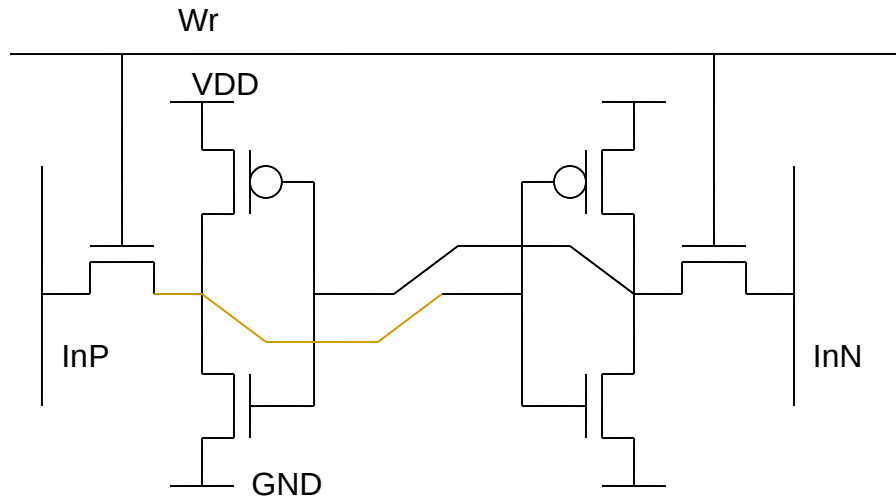
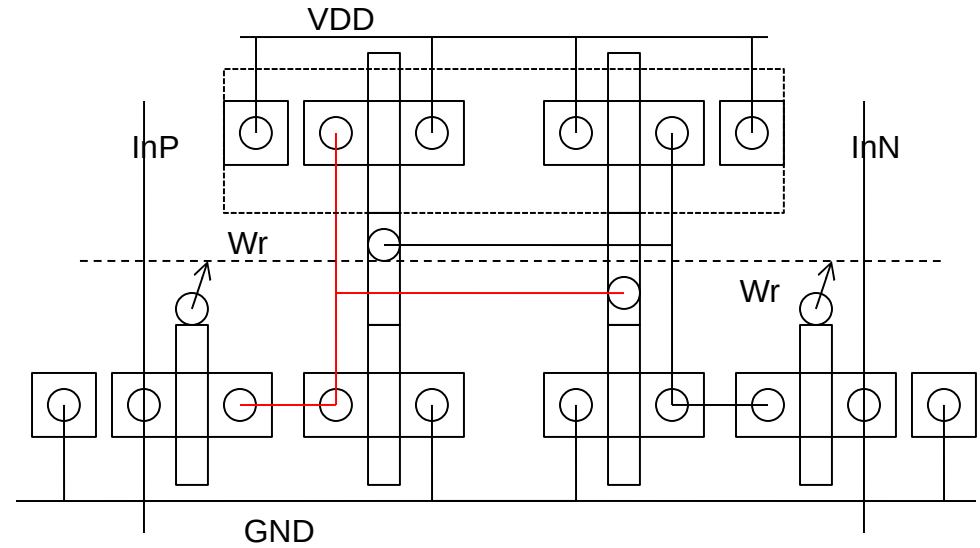
- SRAM



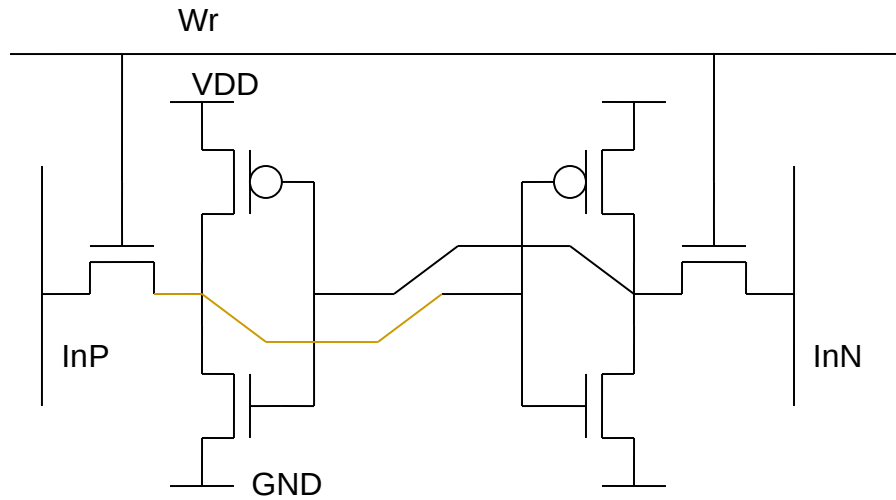
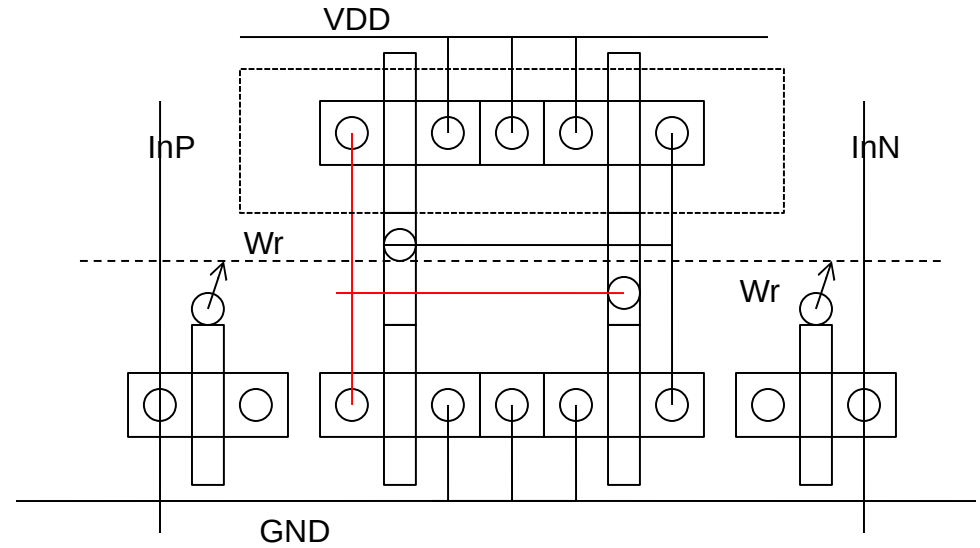
- SRAM



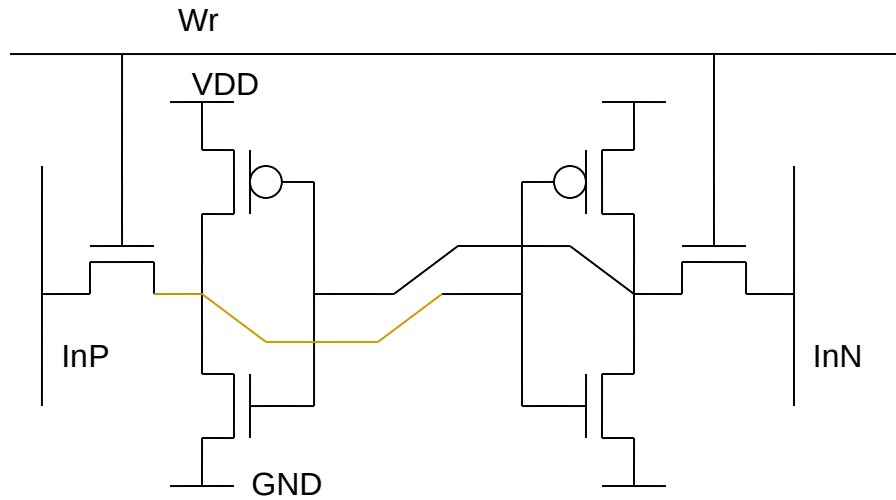
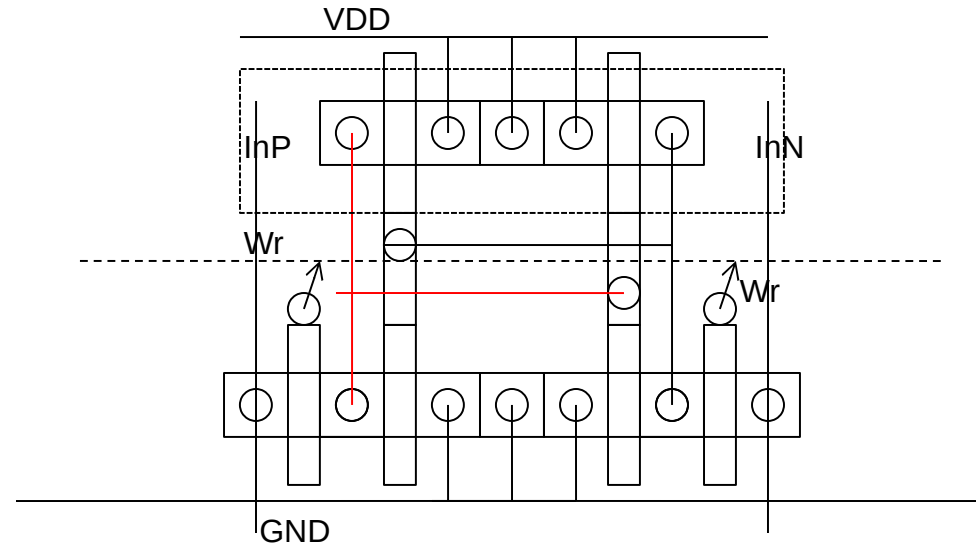
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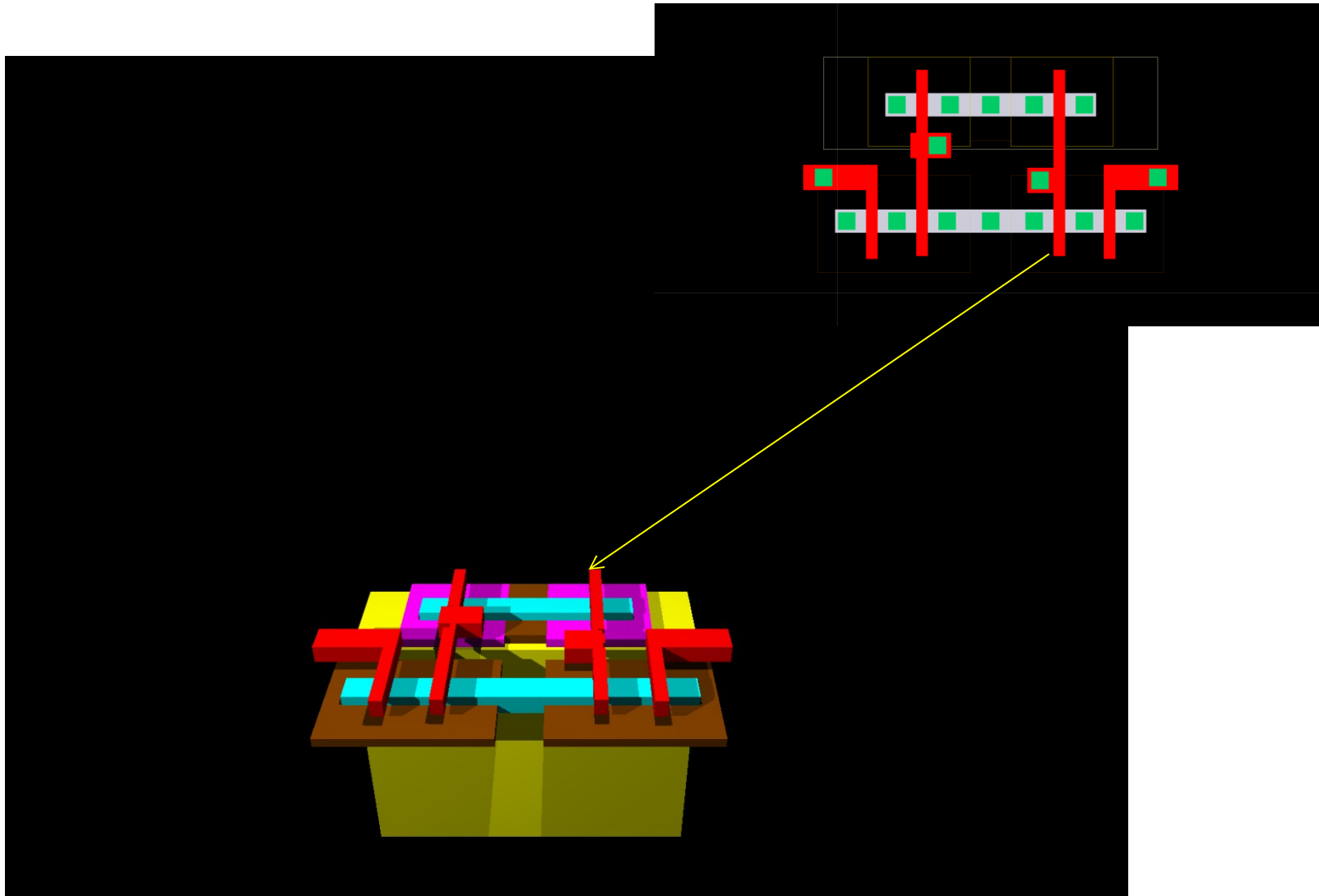
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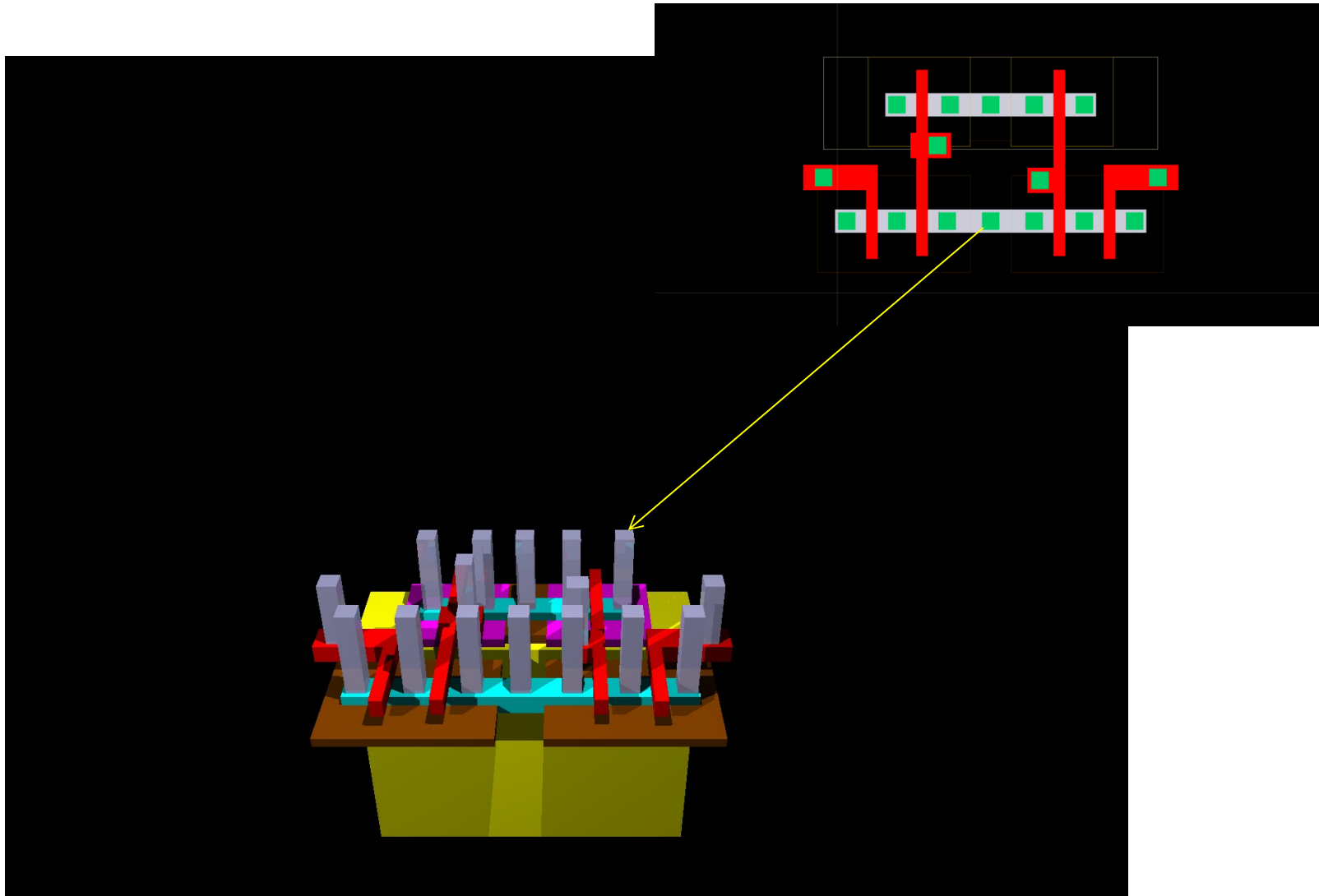
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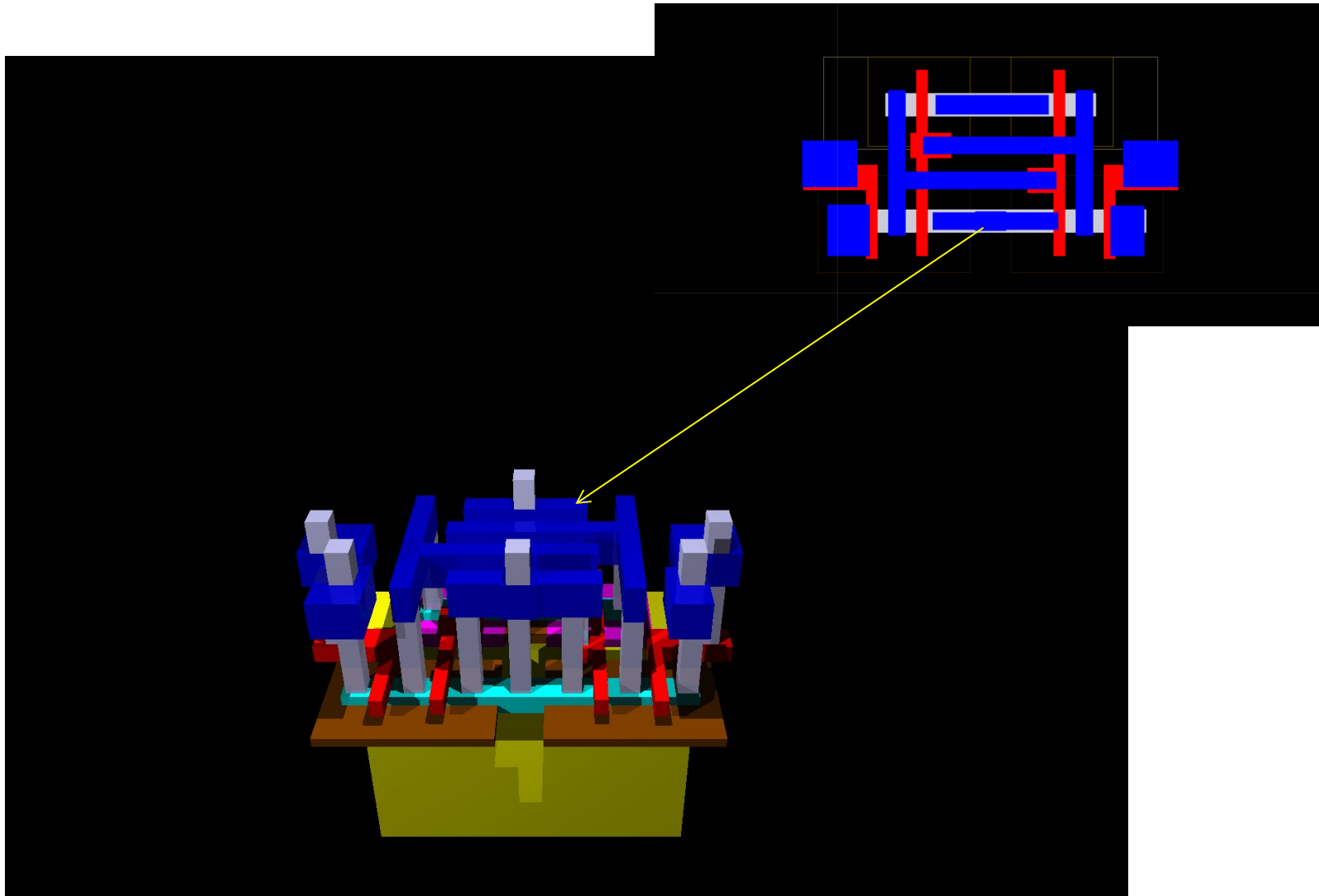
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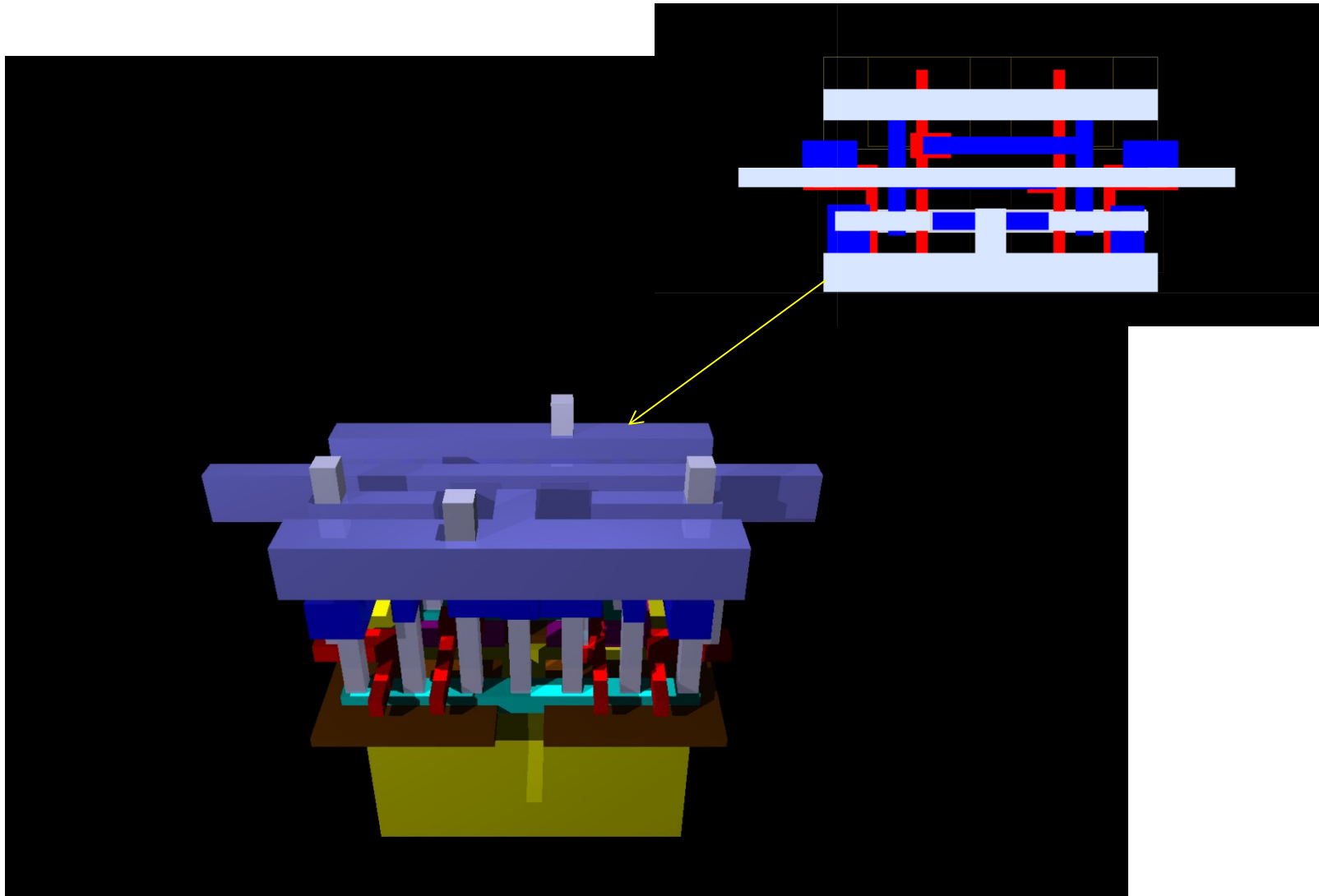
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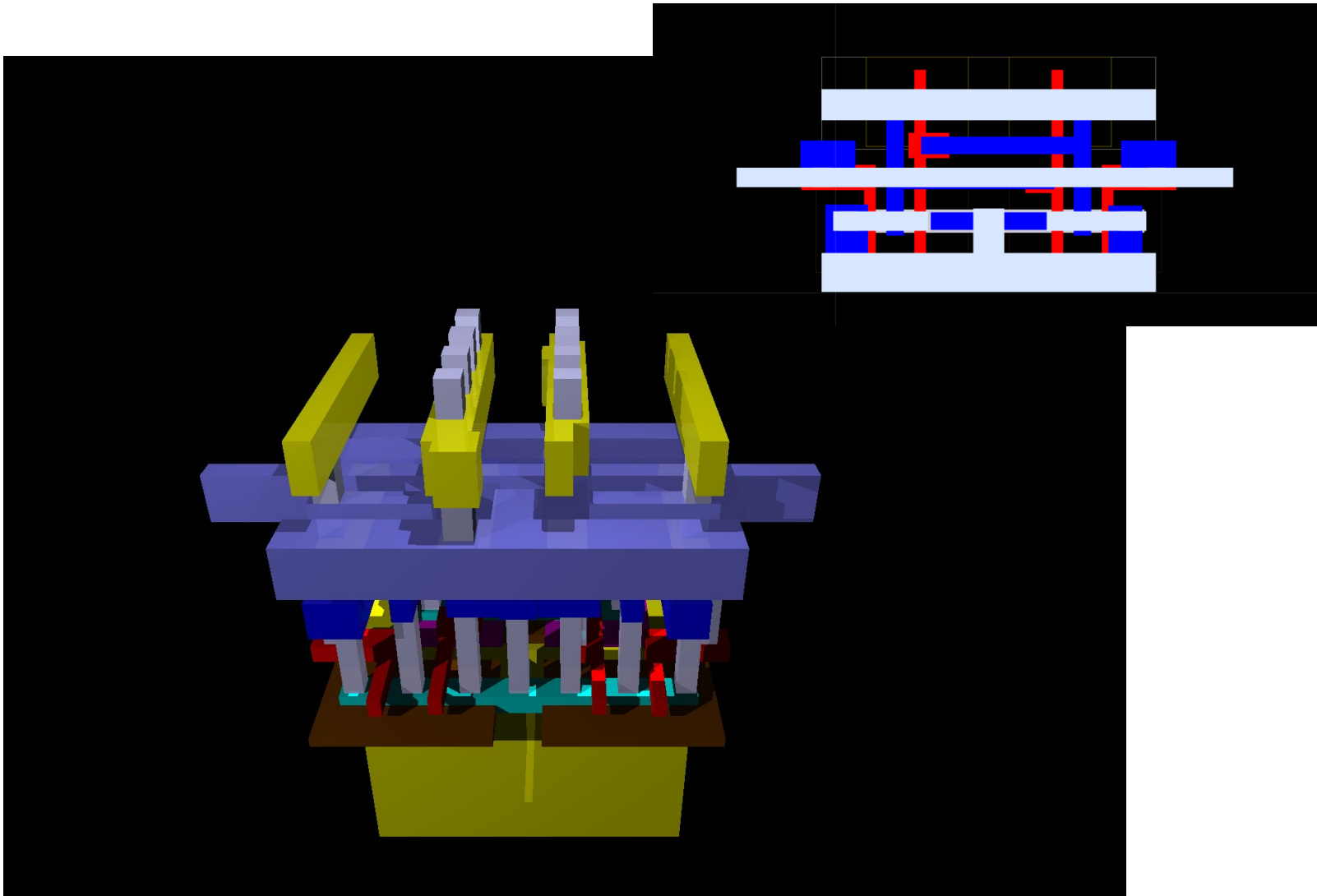
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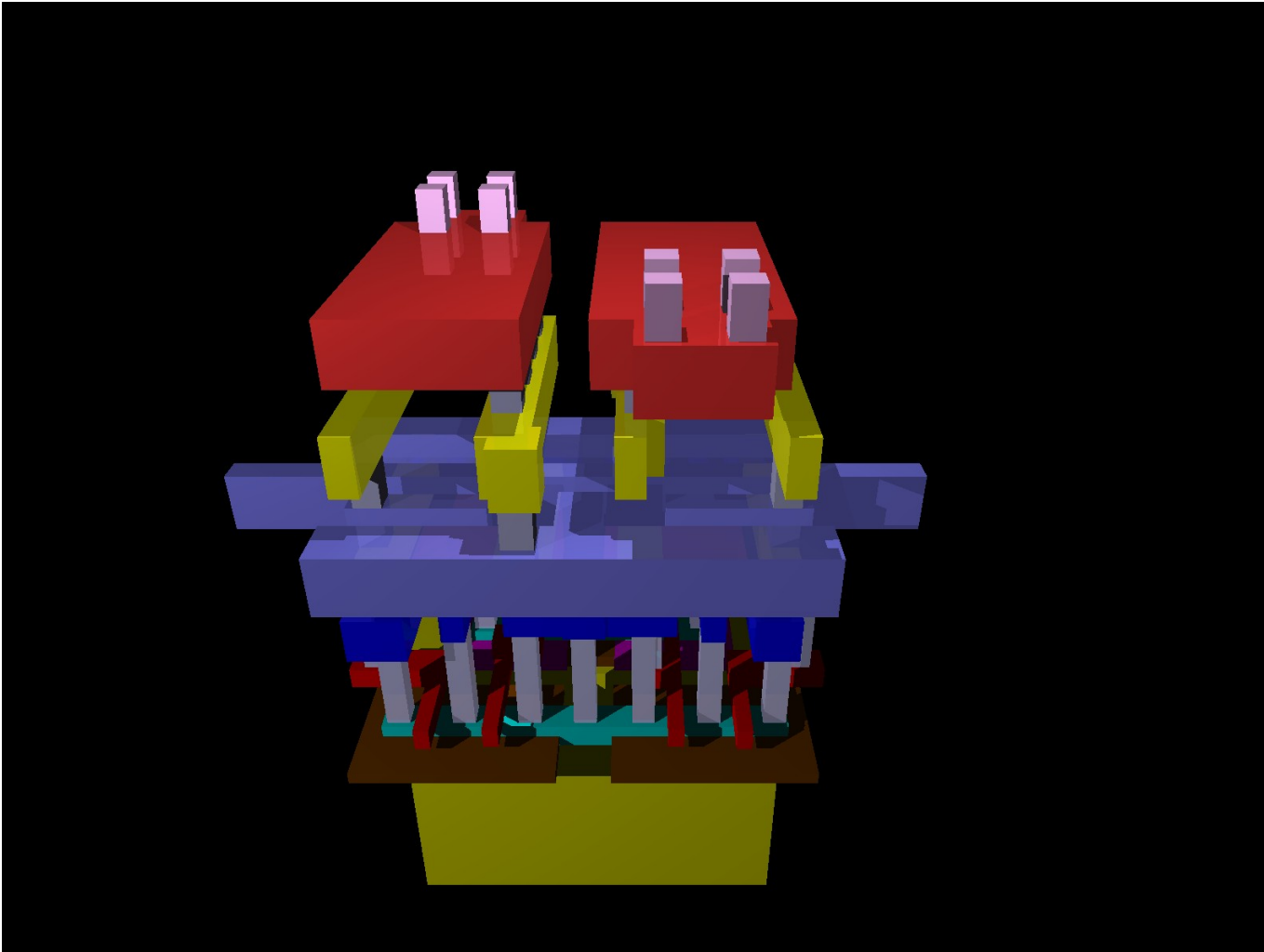
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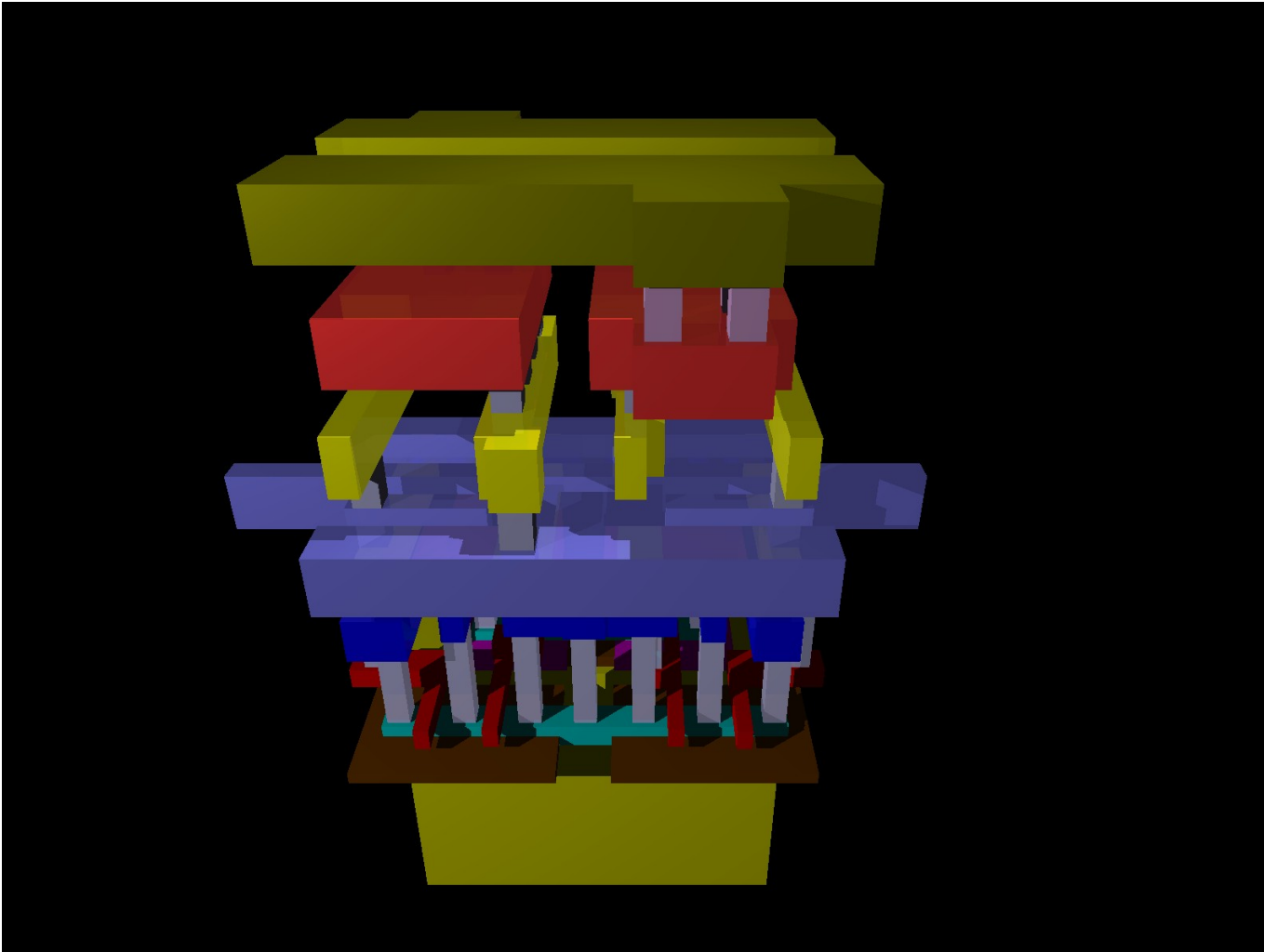
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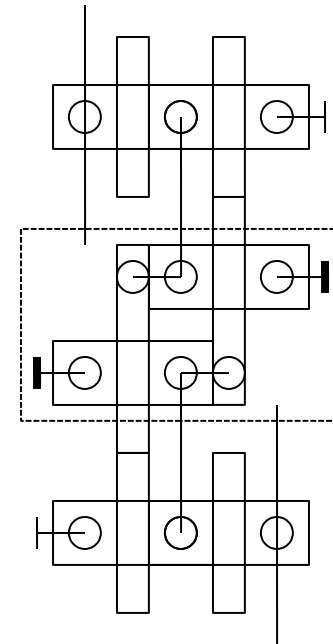
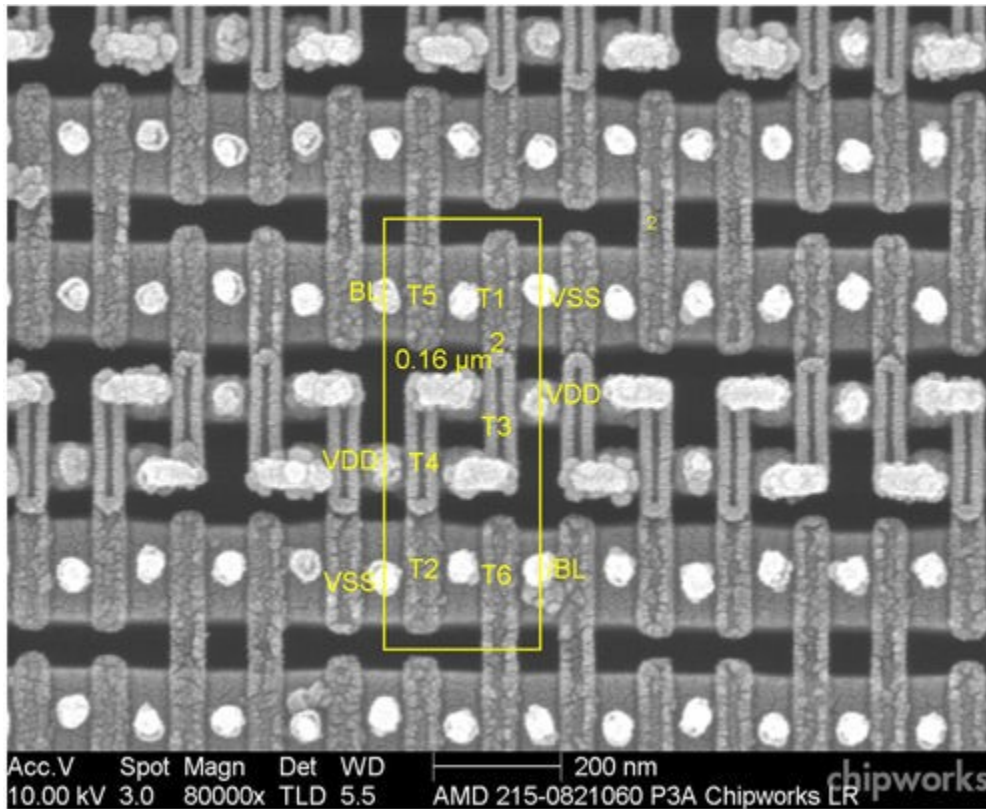
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- ...

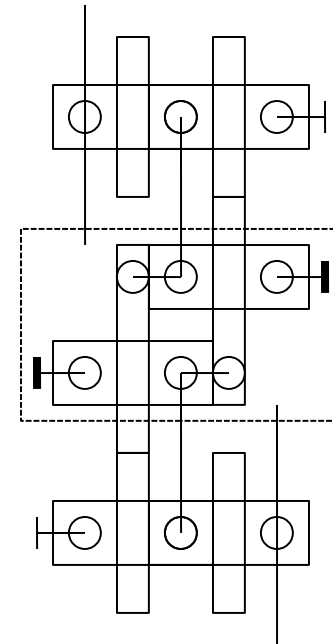


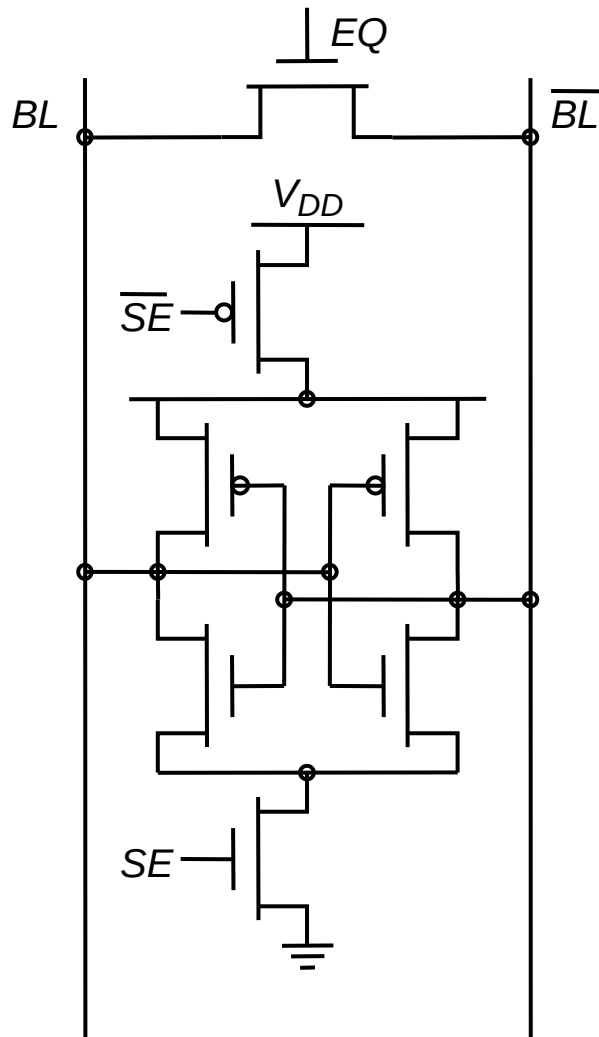
- SRAM



AMD 215-0821060 28 nm HP 6T-SRAM at Poly - Plan View SEM

- SRAM

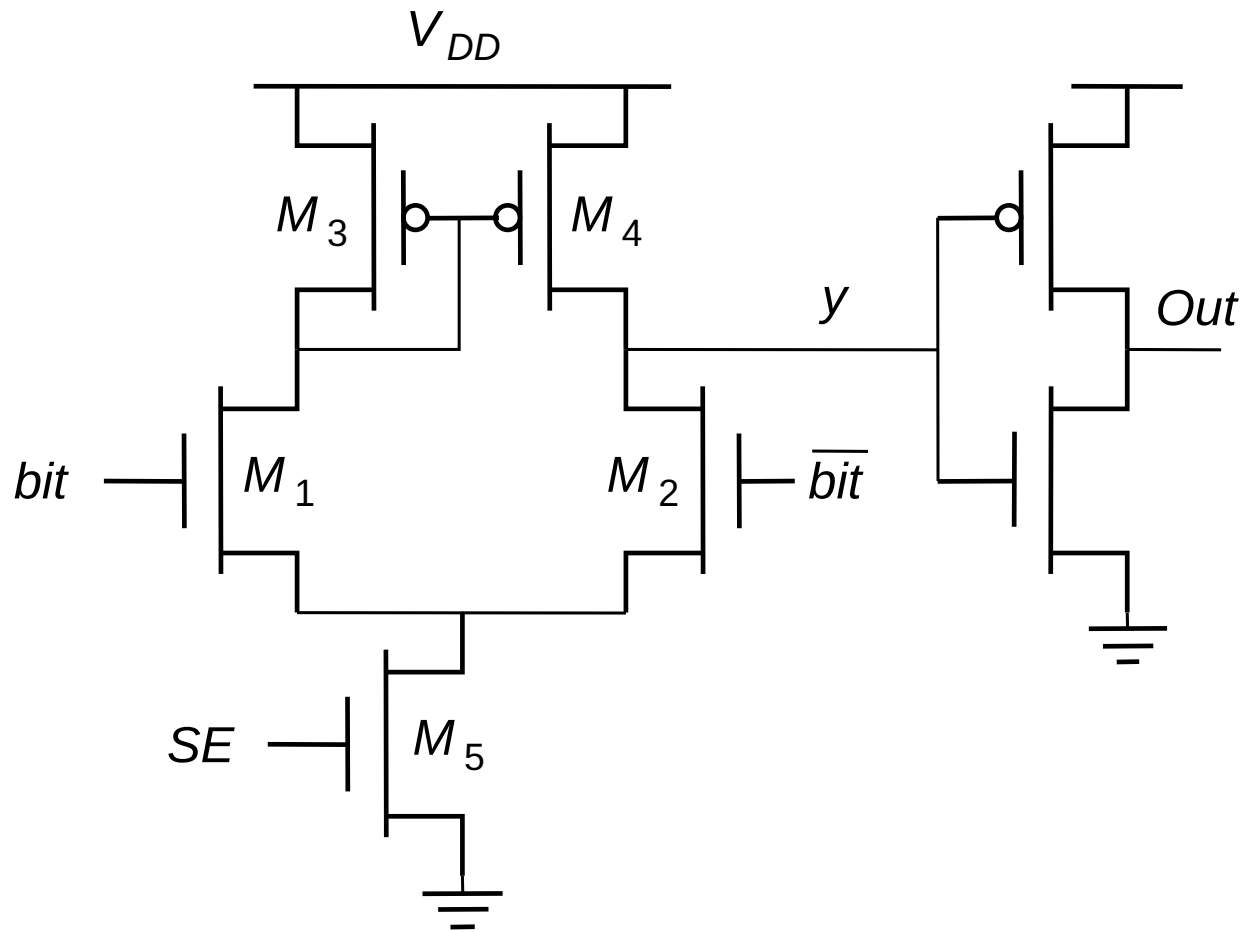


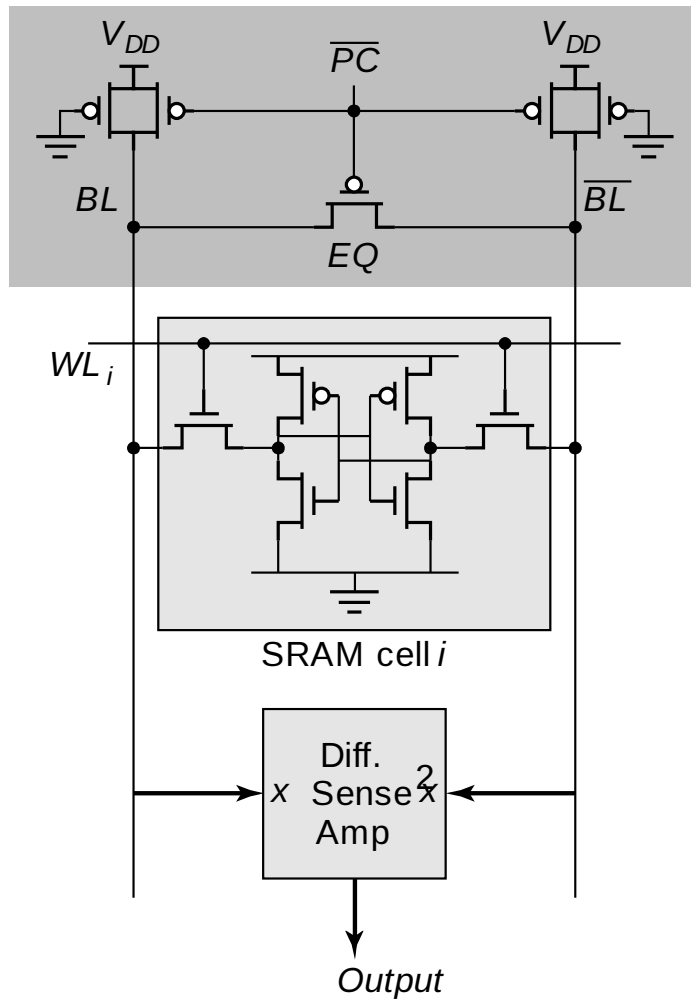


Wird im Schaltungspunkt initialisiert,
d.h. der Zustand ist metastabil

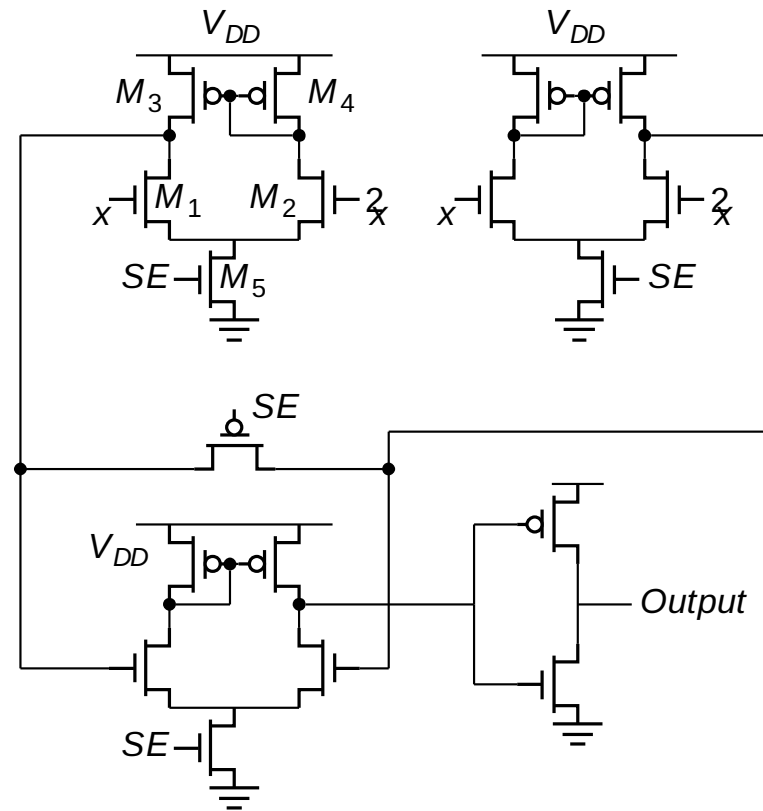
Schnelles Umkippen durch positive
Rückkopplung

SE selektiert den Verstärker

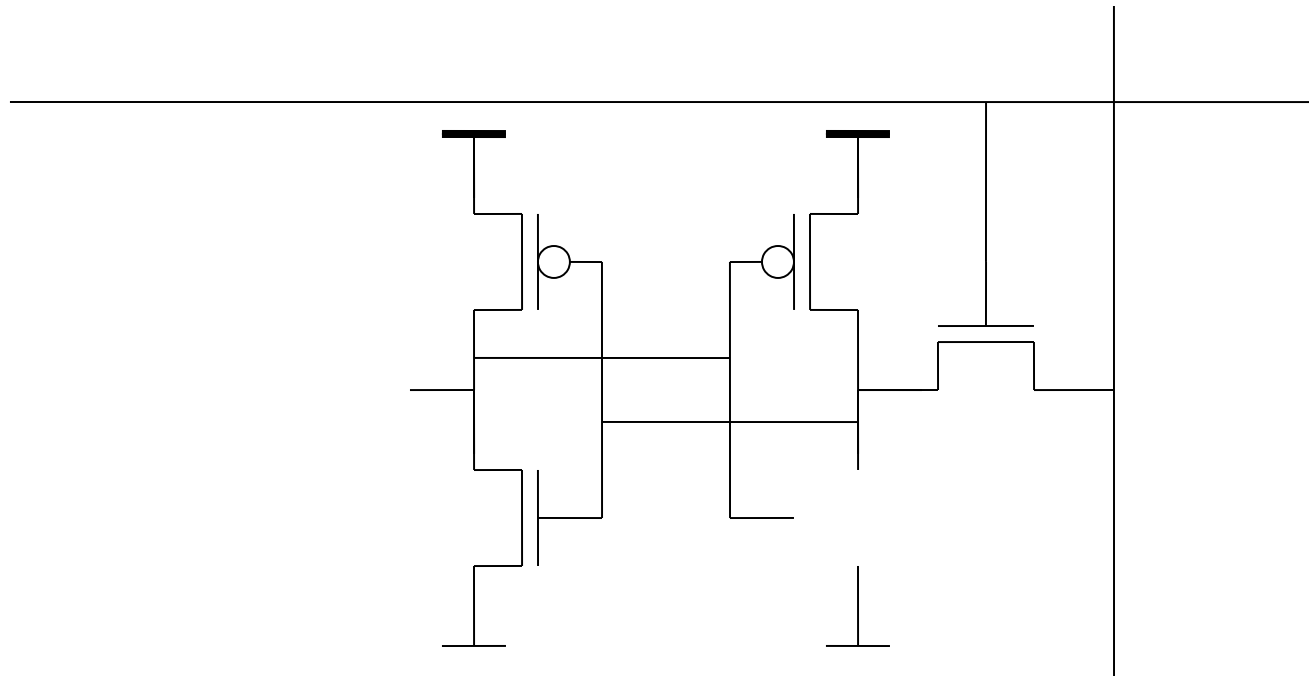


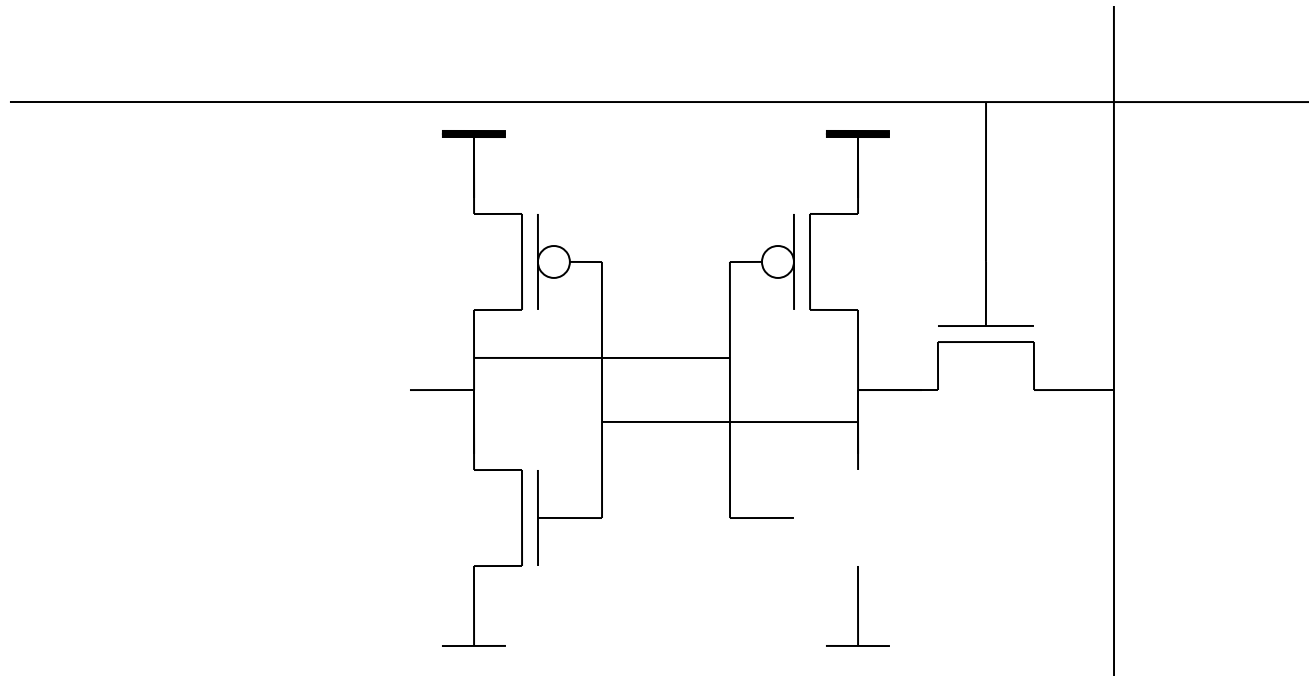


(a) SRAM sensing scheme



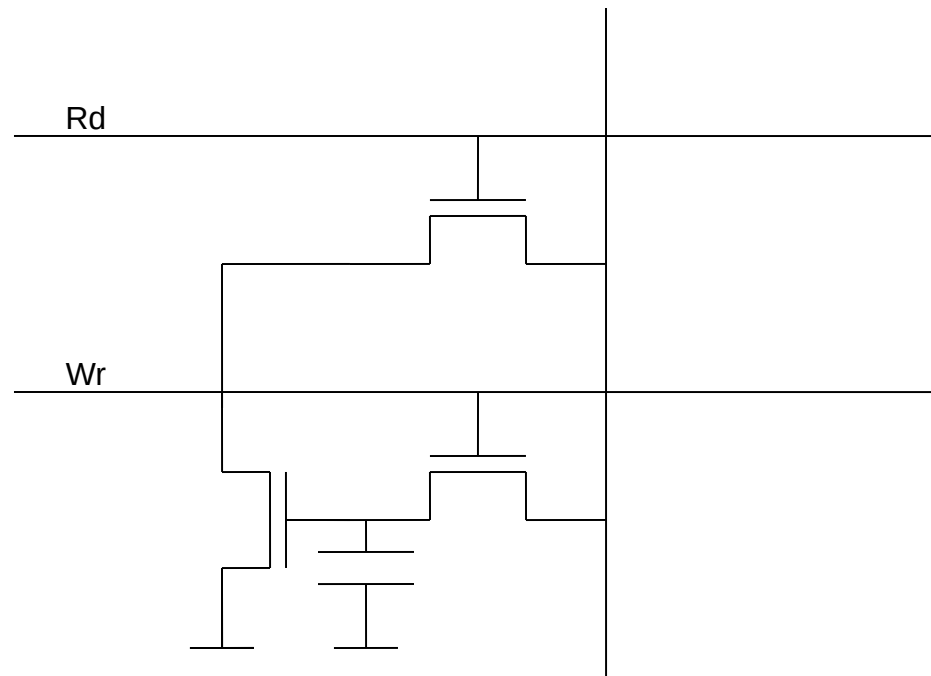
(b) two stage differential amplifier



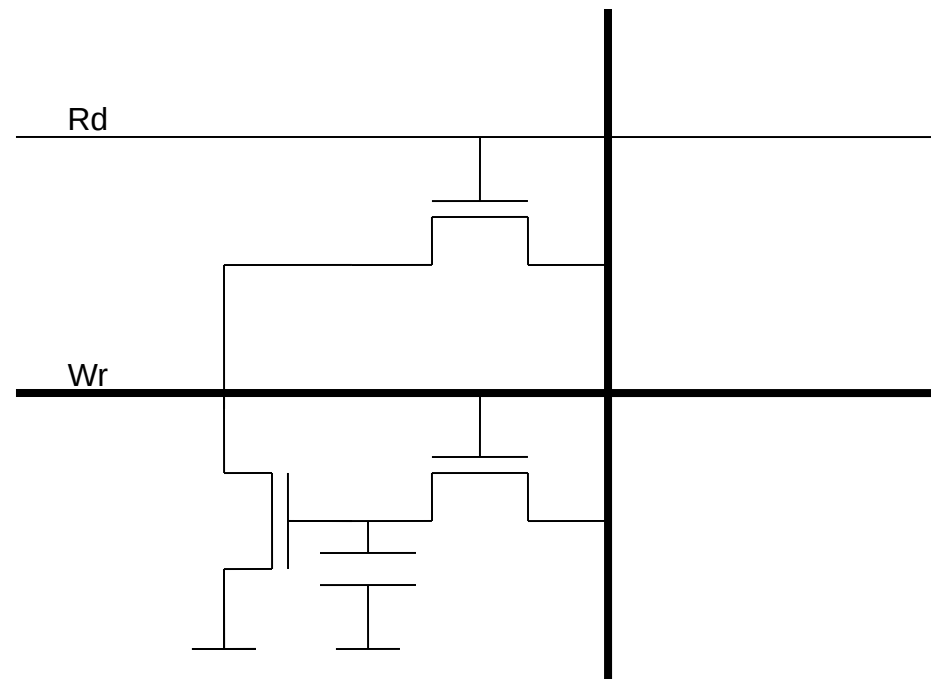


DRAM

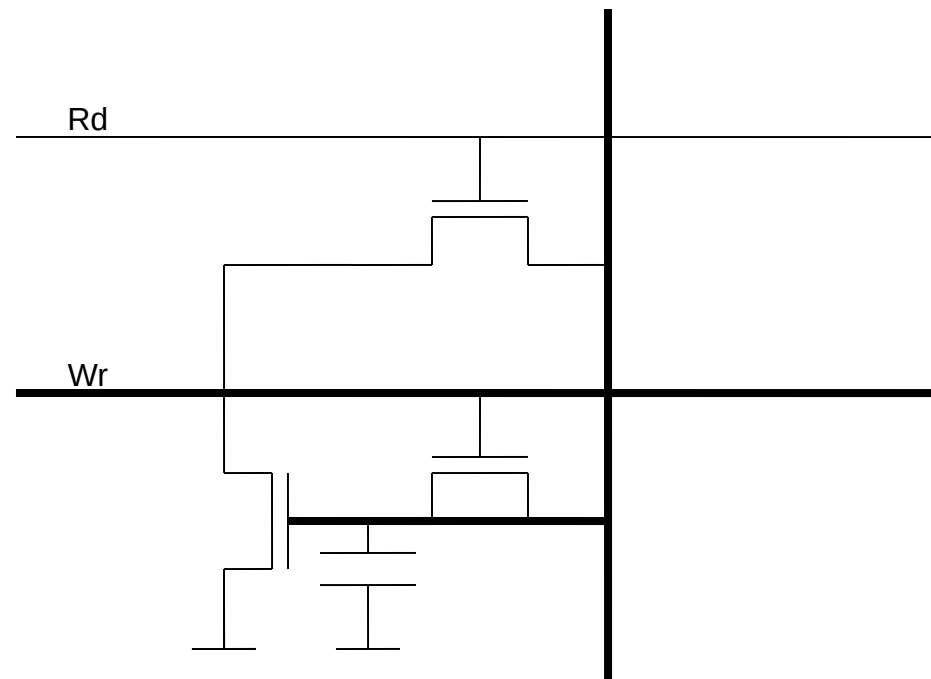
- DRAM



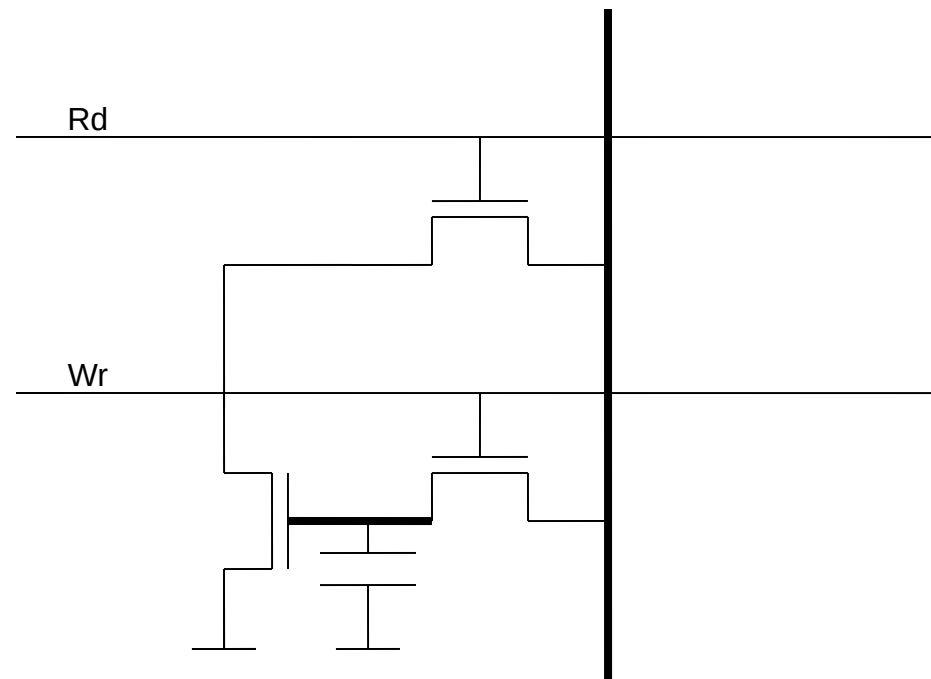
- DRAM



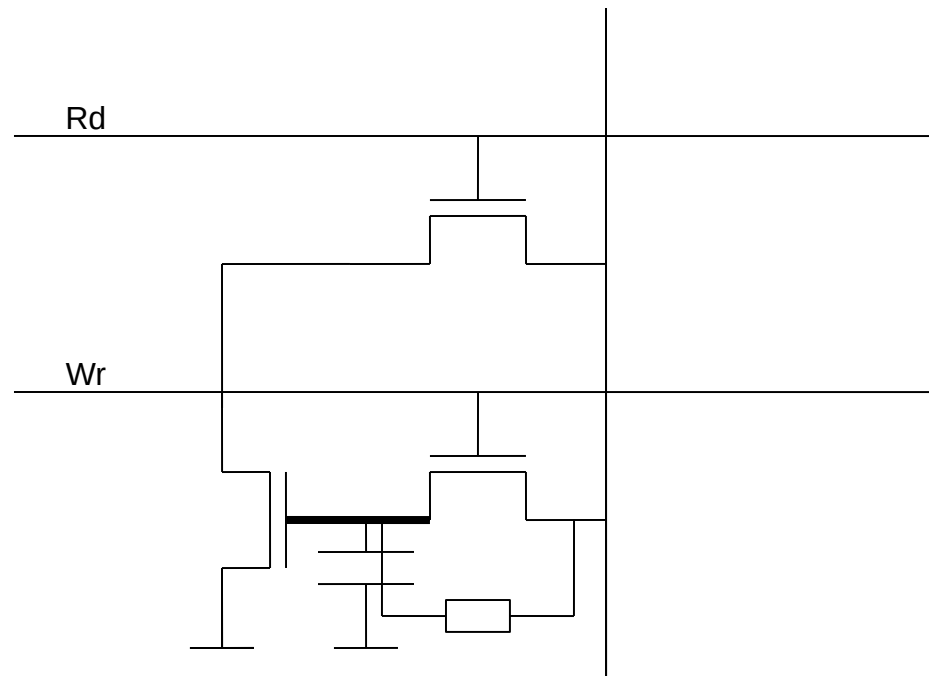
- DRAM



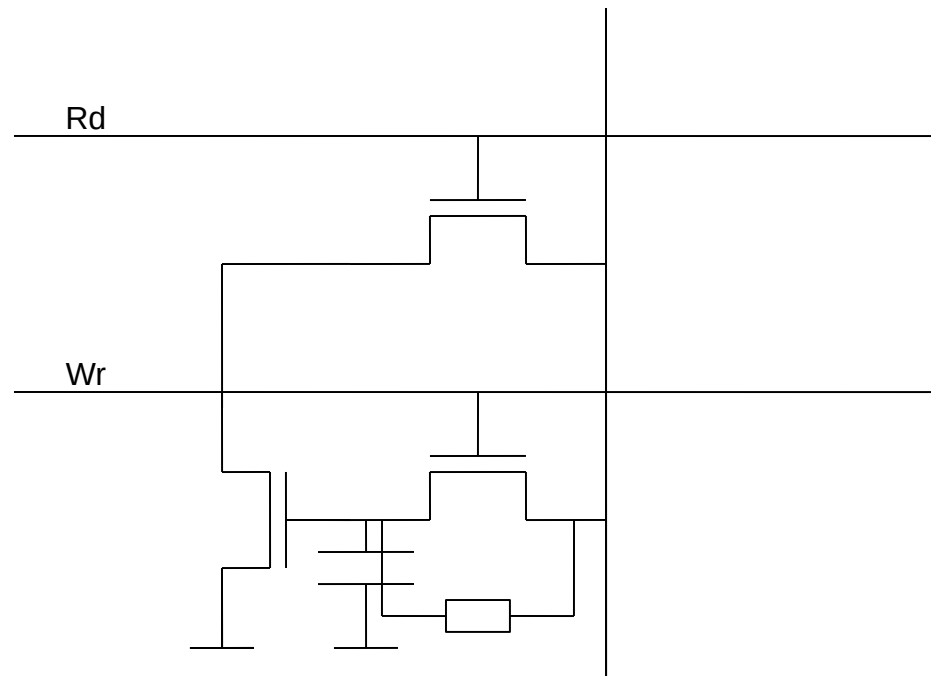
- DRAM



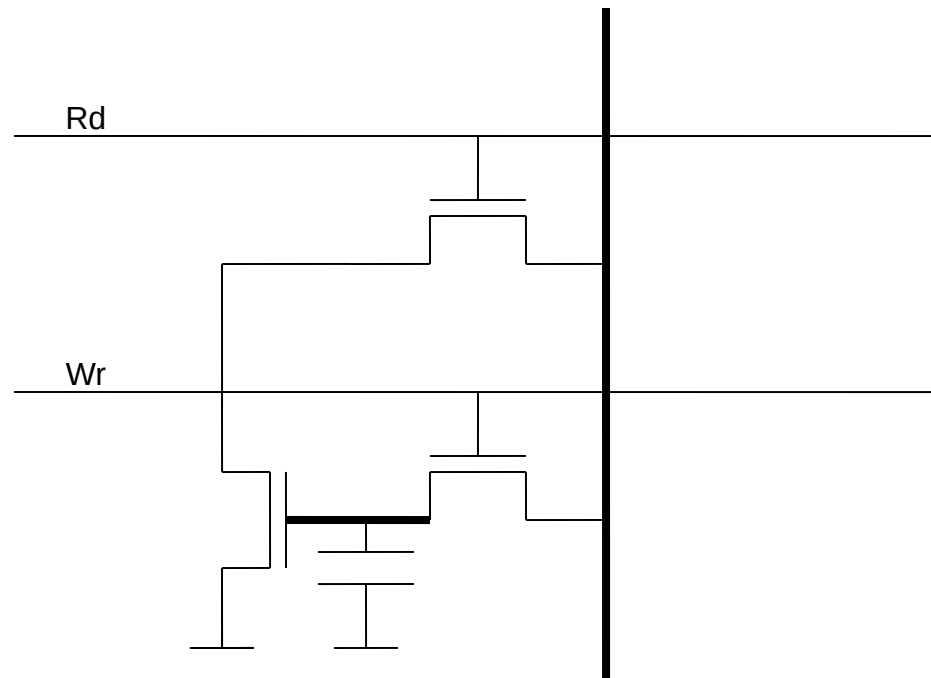
- DRAM



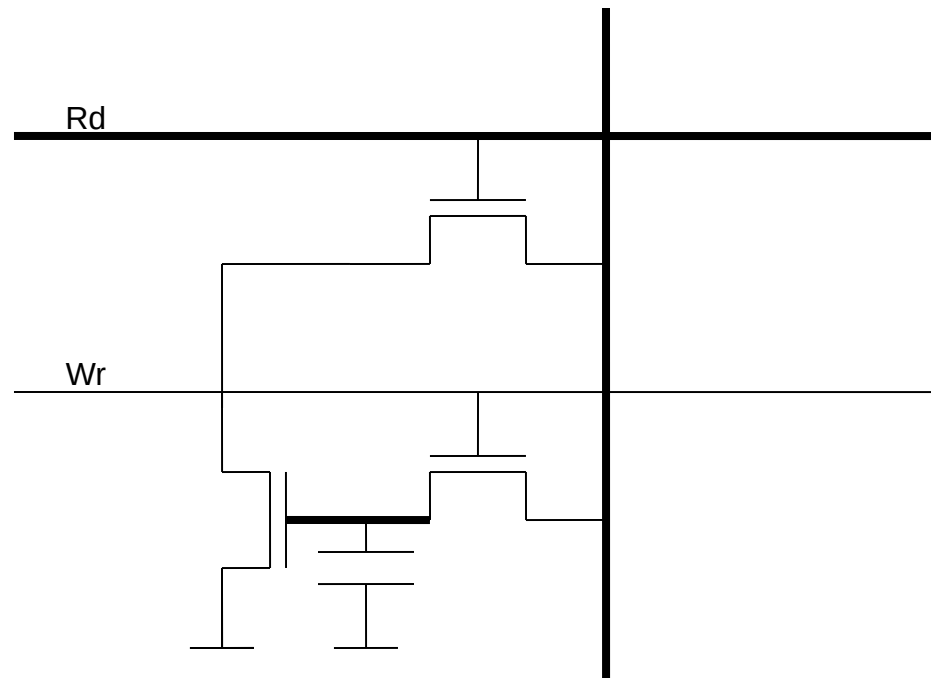
- DRAM



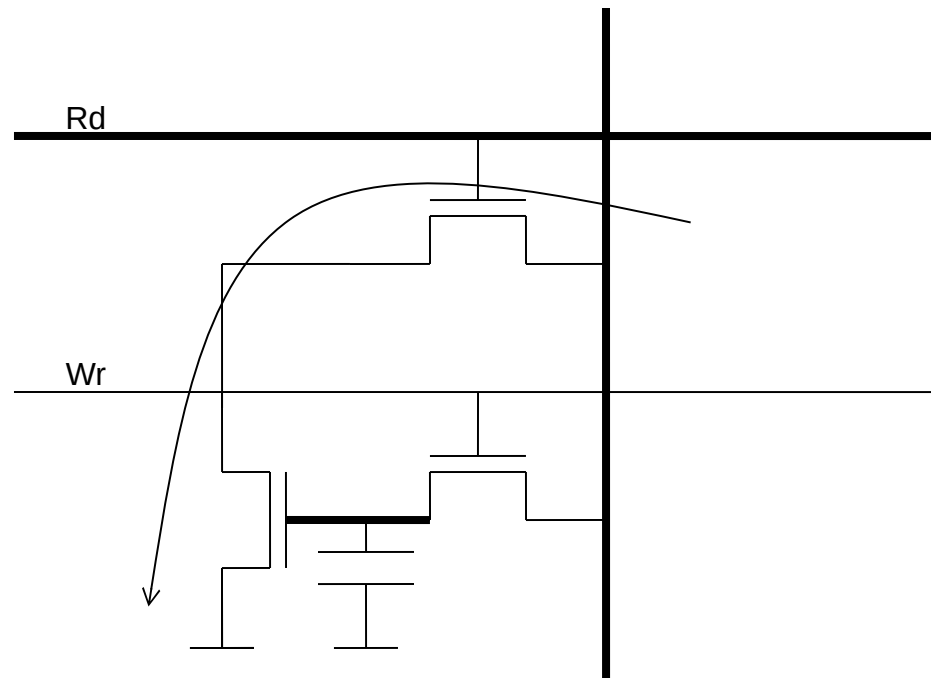
- DRAM



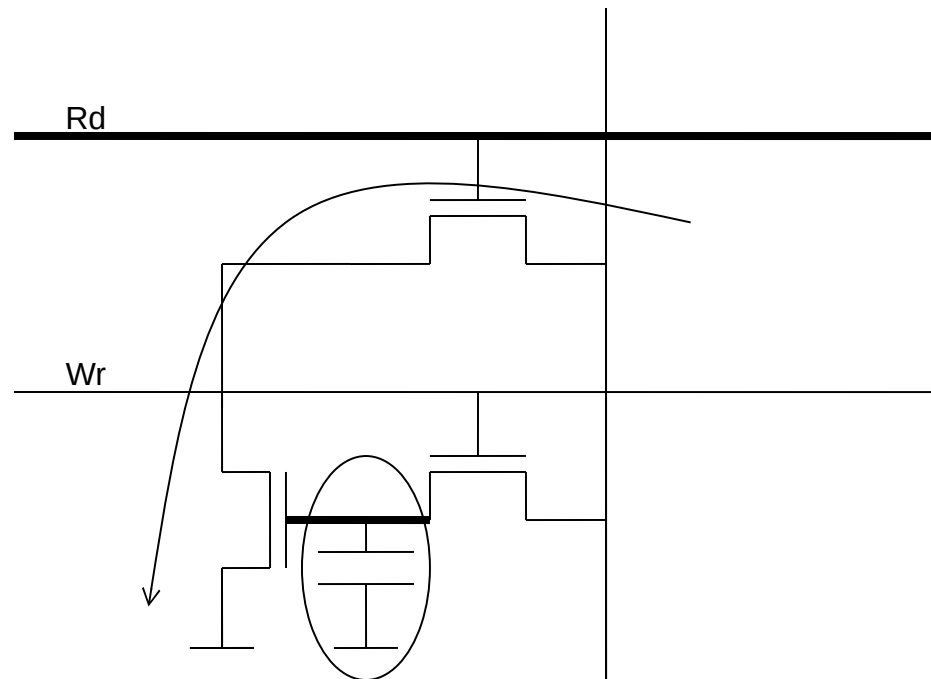
- DRAM



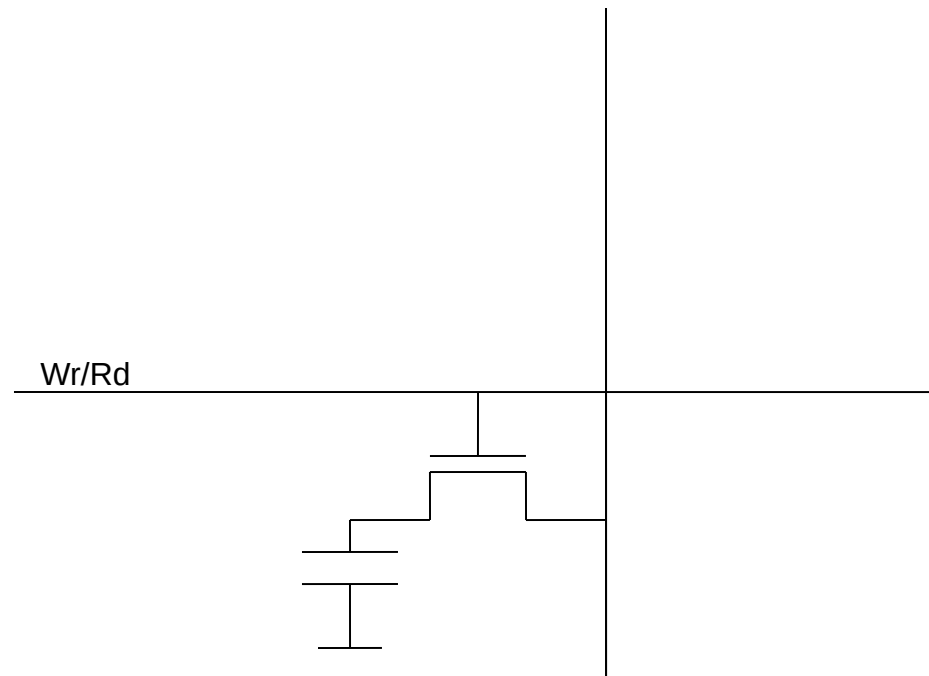
- DRAM



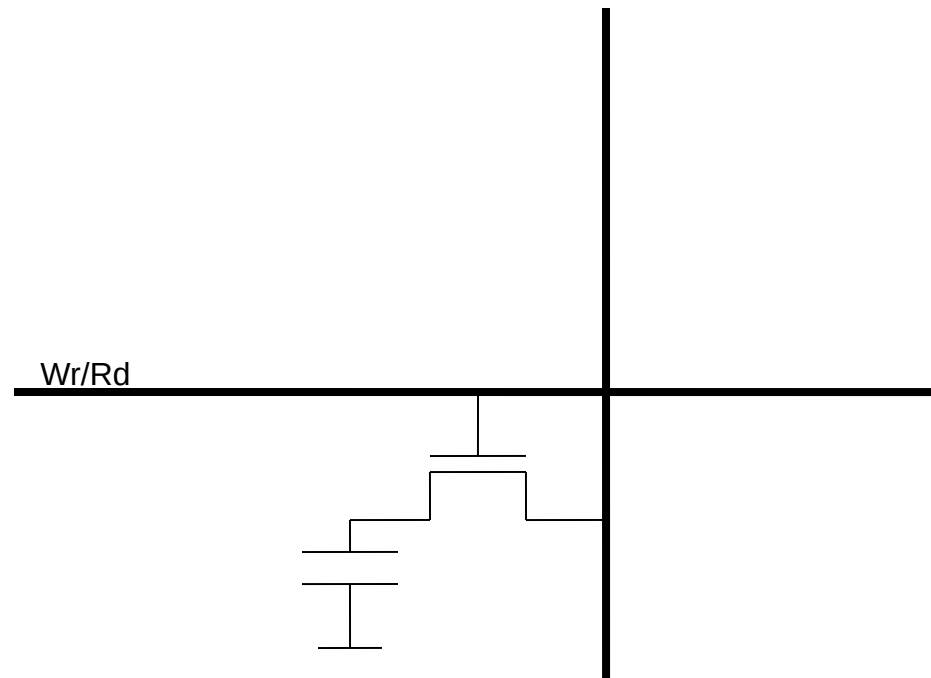
- DRAM



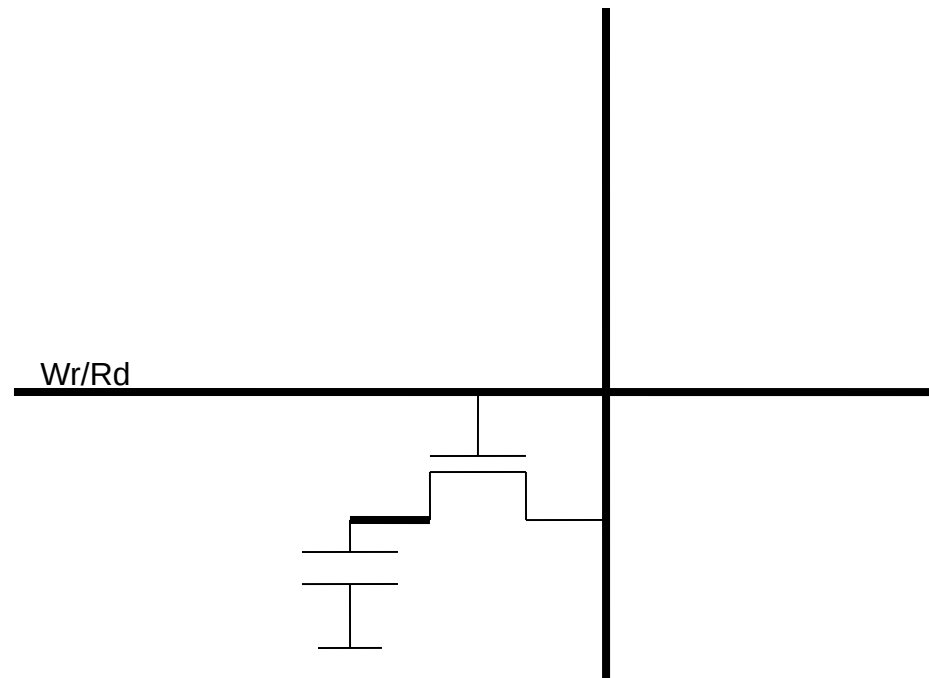
- 1 transistor DRAM



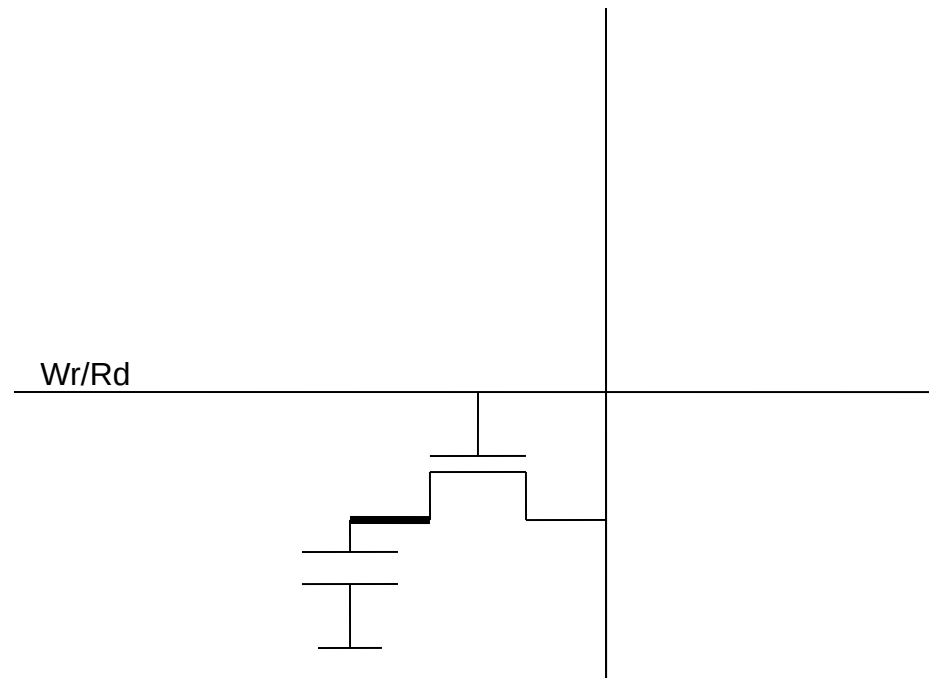
- 1 transistor DRAM



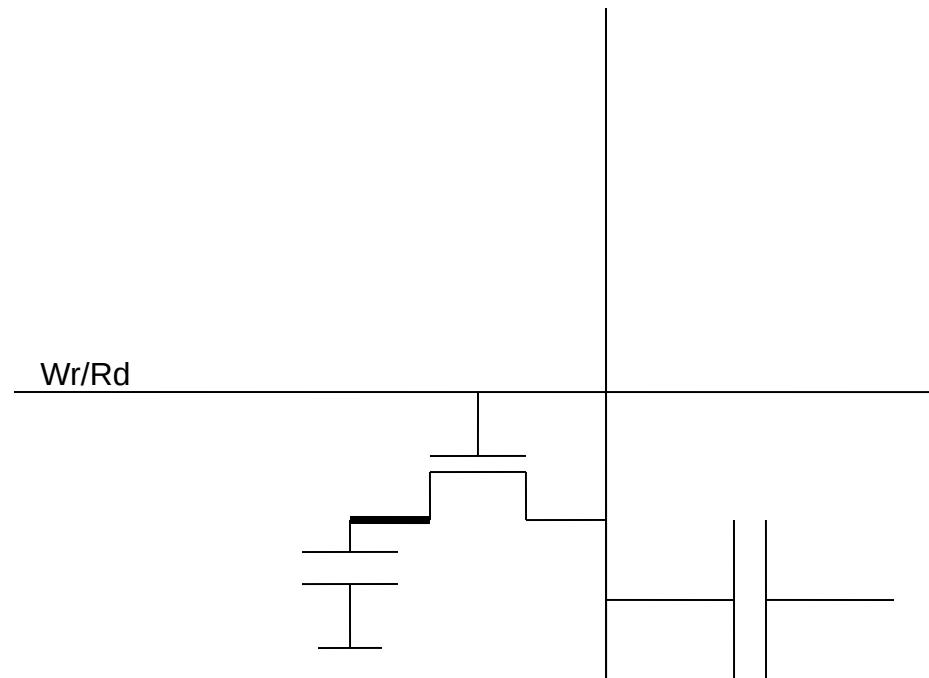
- 1 transistor DRAM



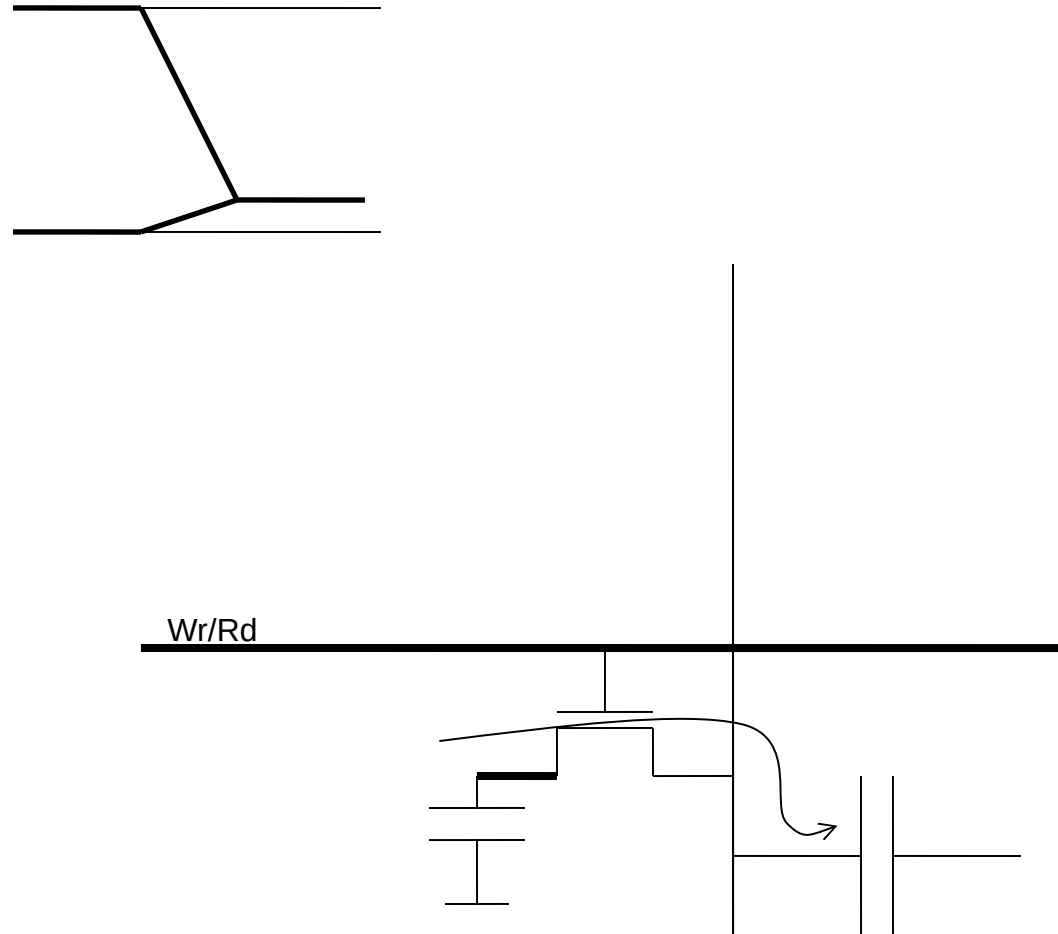
- 1 transistor DRAM



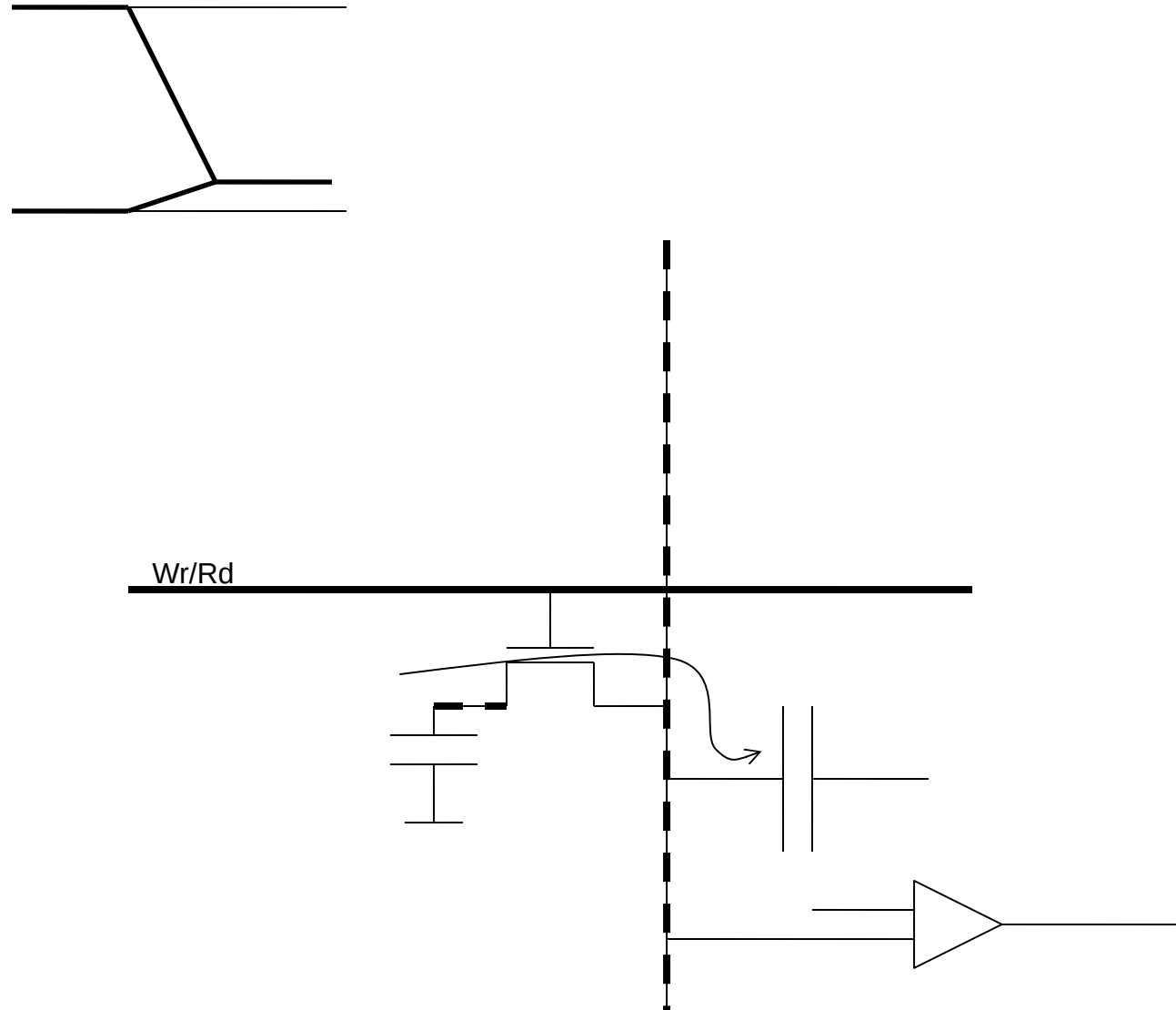
- 1 transistor DRAM



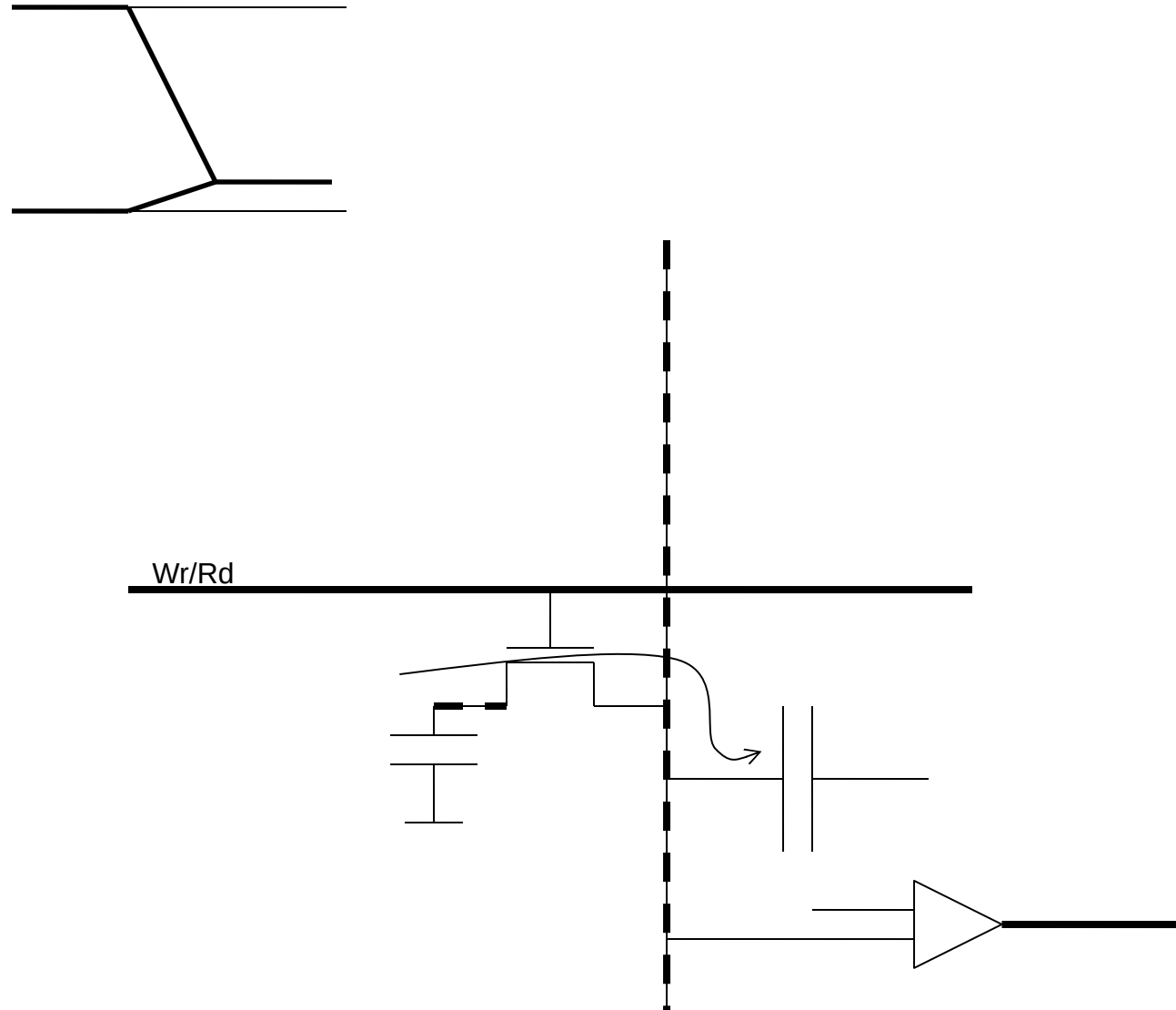
- 1 transistor DRAM



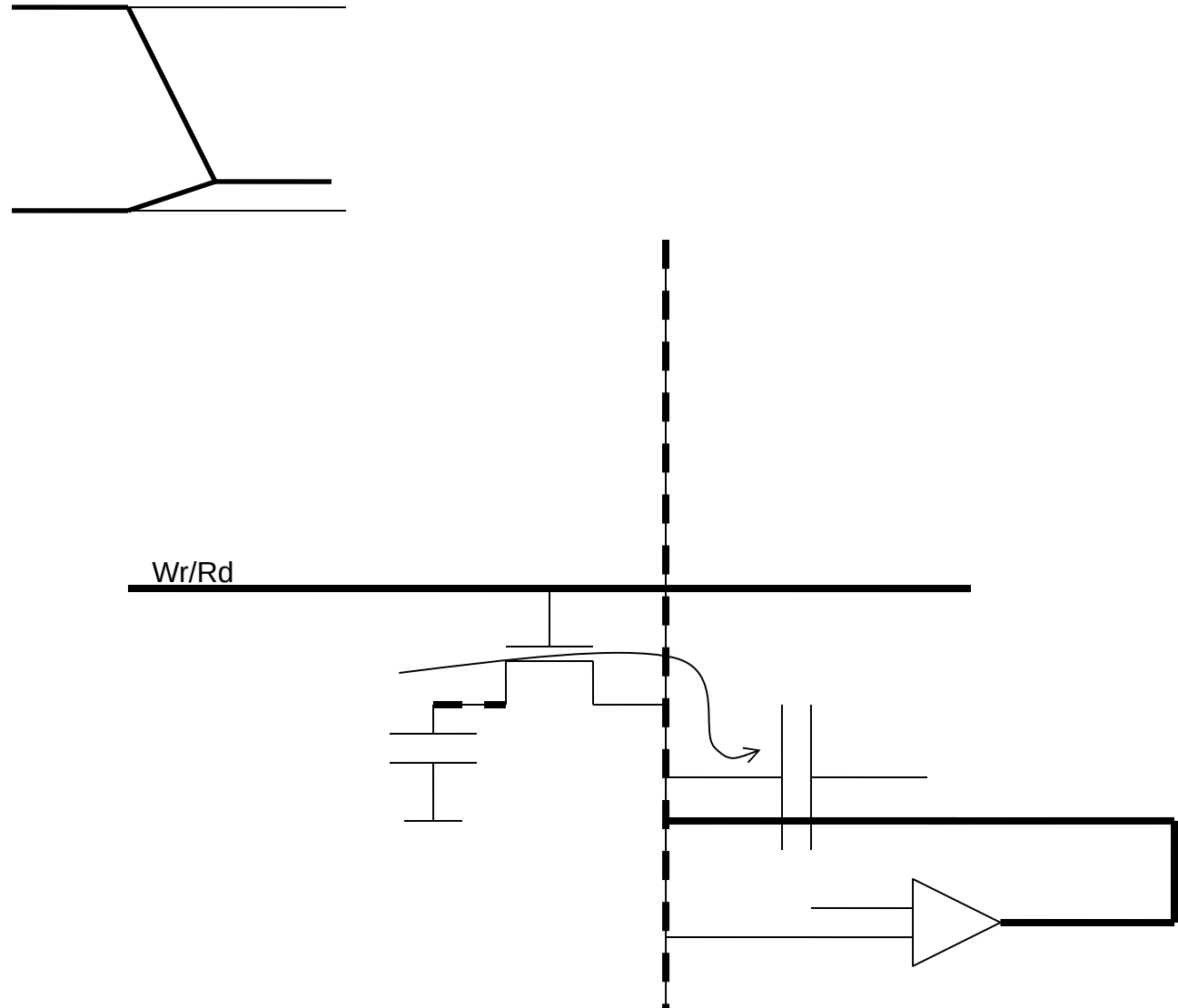
- 1 transistor DRAM



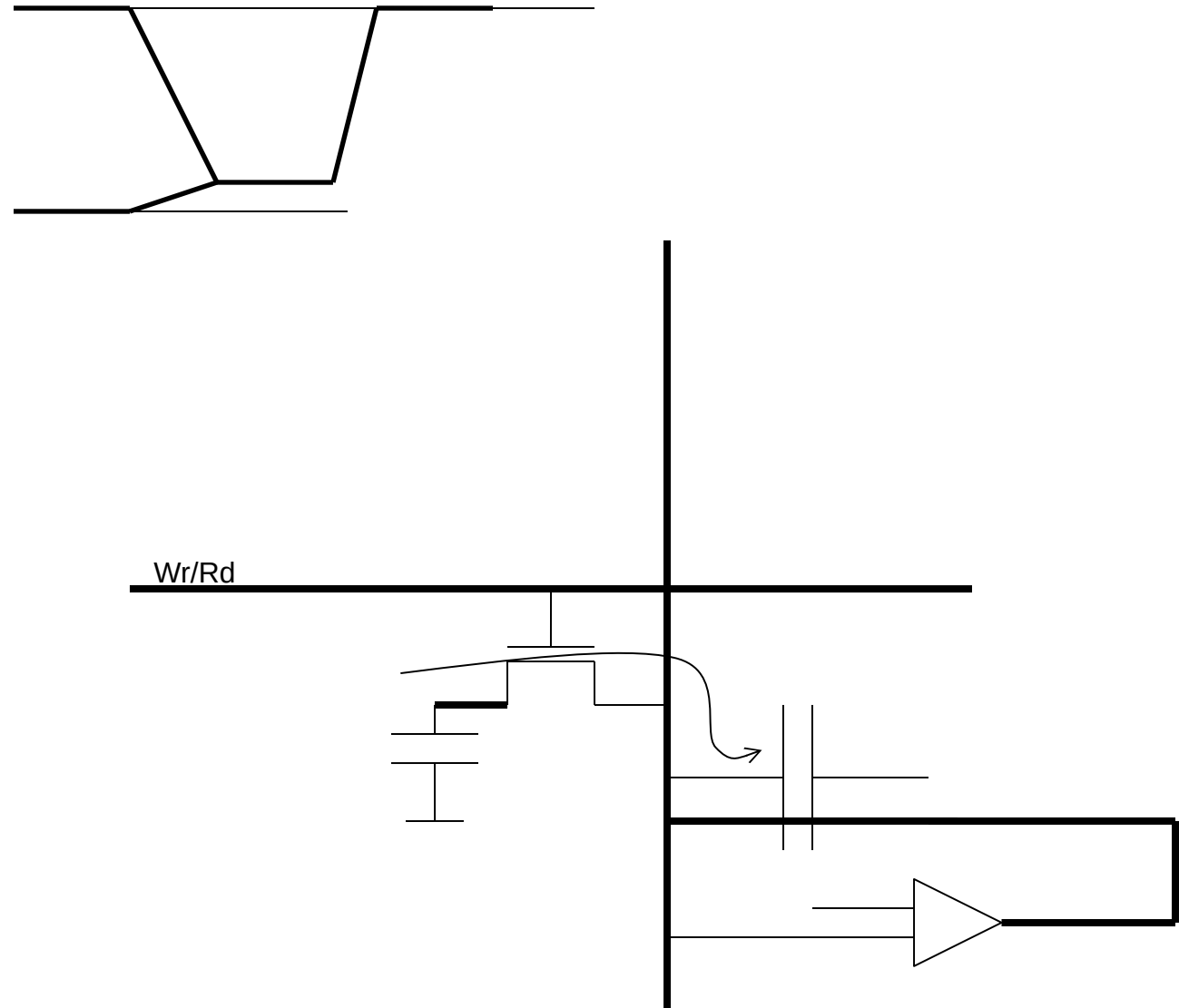
- 1 transistor DRAM



- 1 transistor DRAM



- 1 transistor DRAM



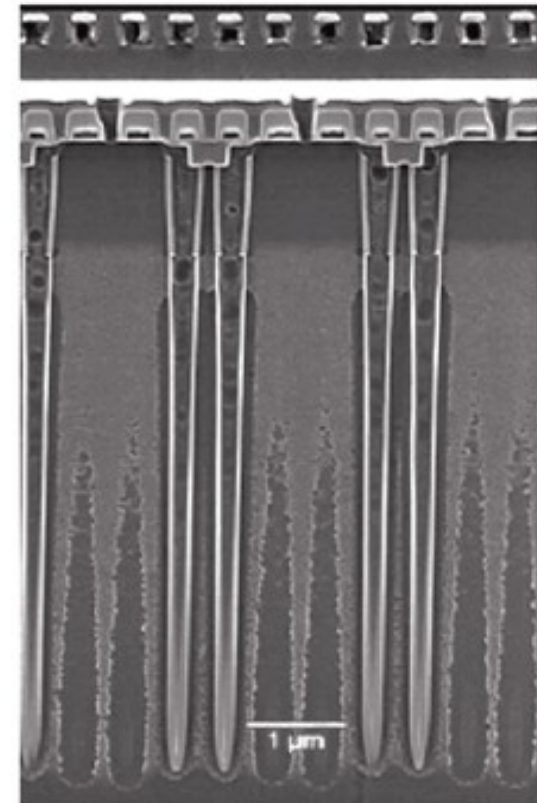
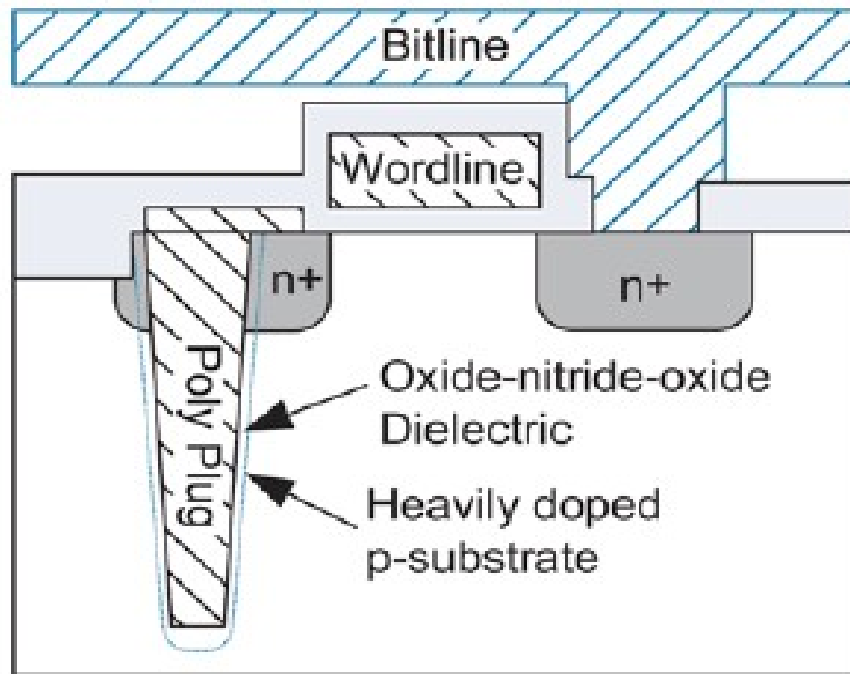
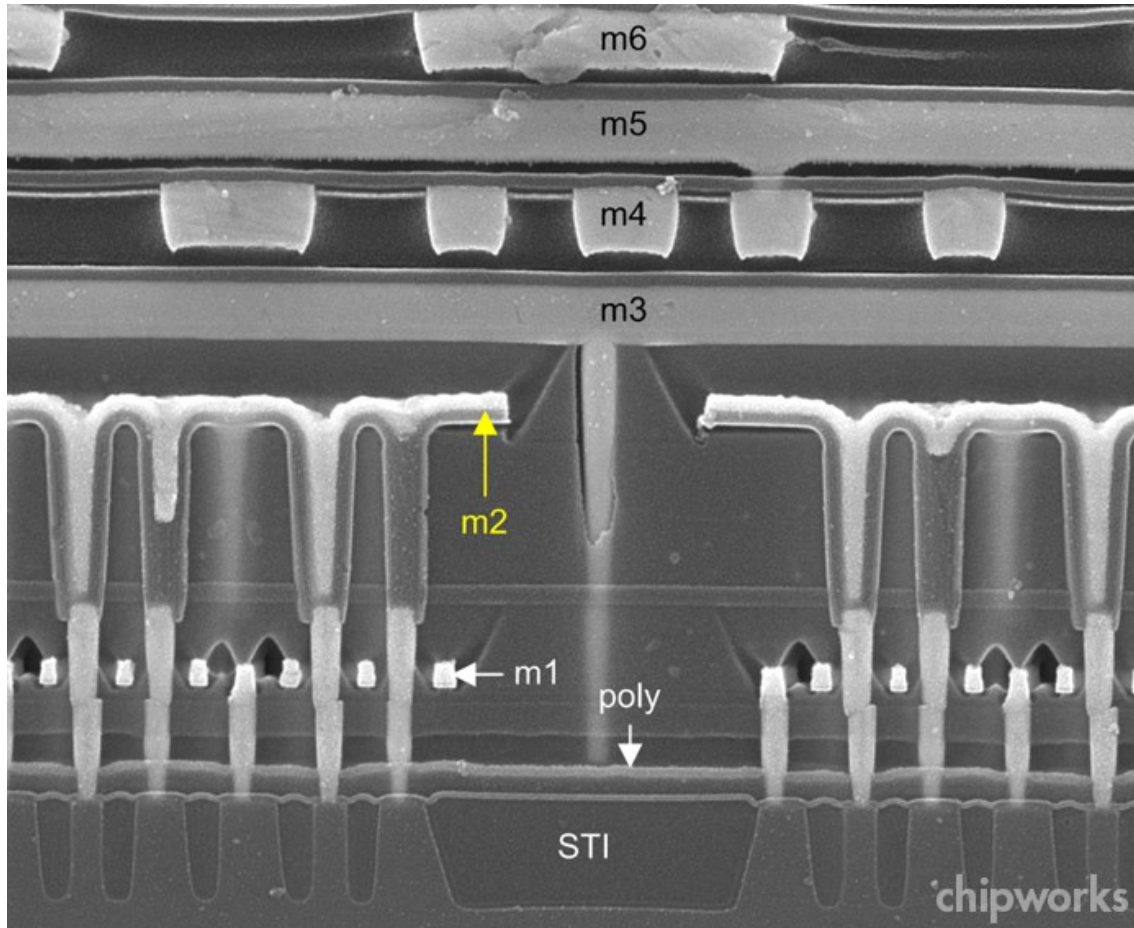


FIG 11.27 Trench capacitor

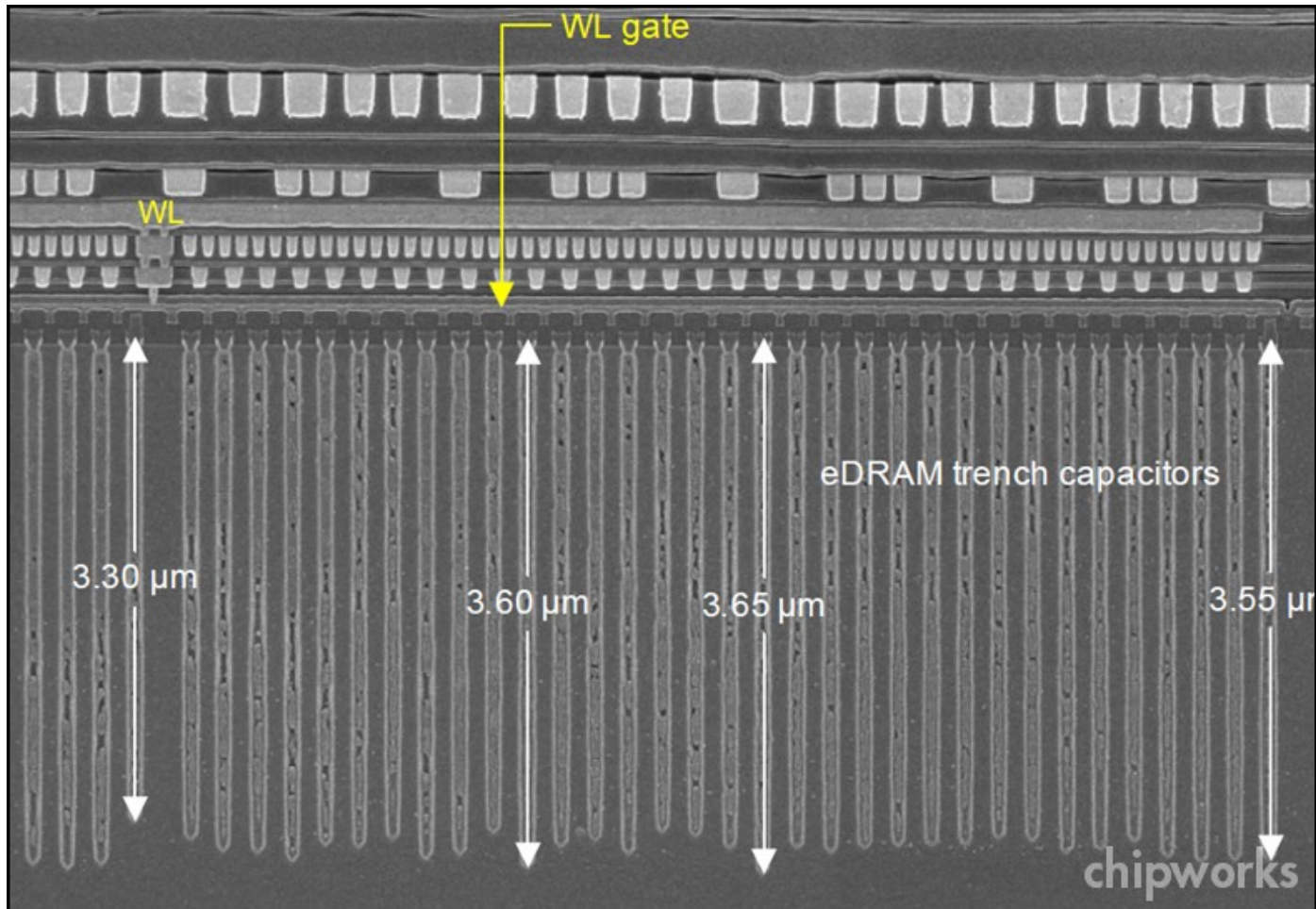
- DRAM



Embedded DRAM in Nintendo Wii U GPU fabbed by Renesas (45-nm)

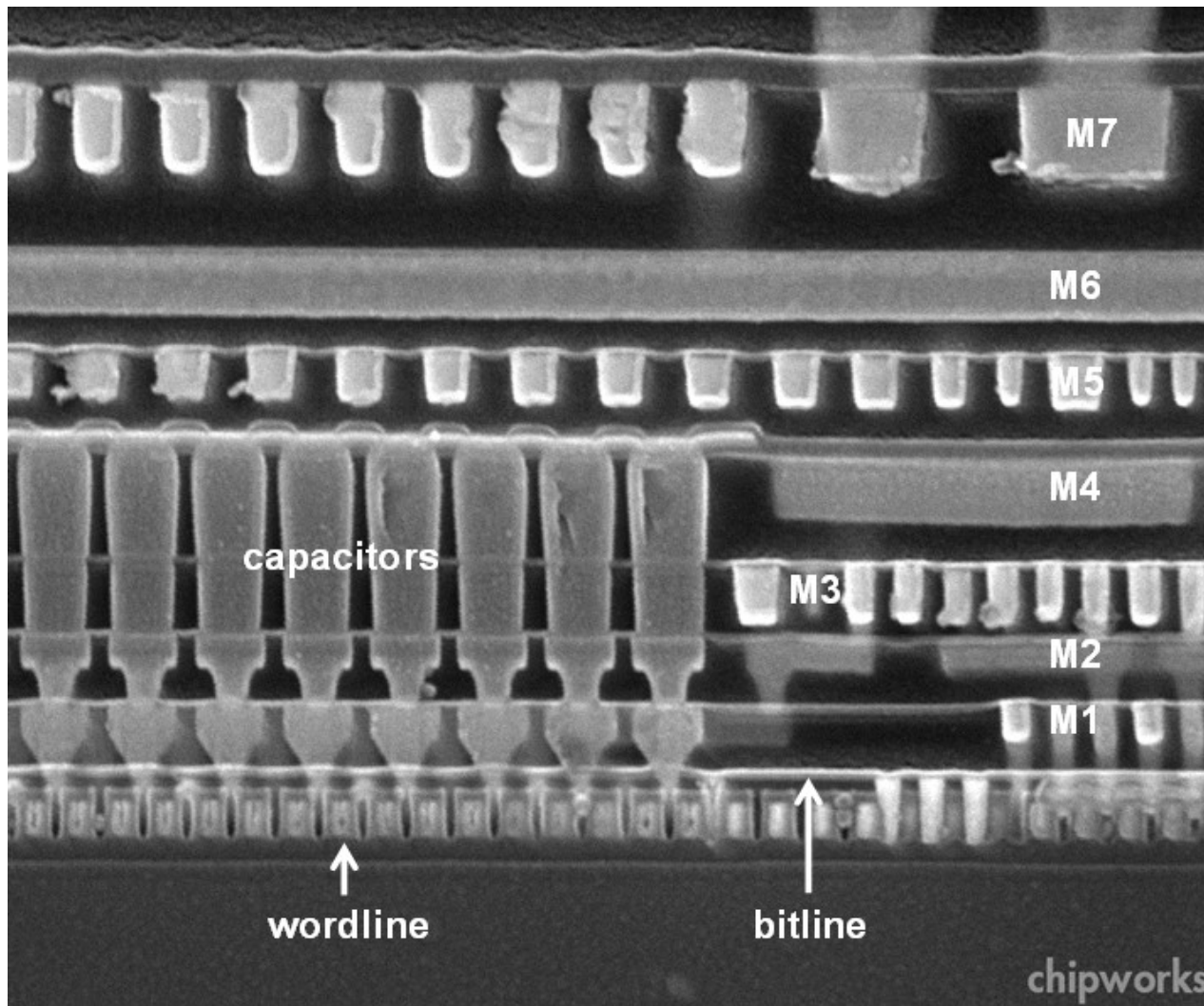
<http://chipworksrealchips.blogspot.de/2014/02/intels-e-dram-shows-up-in-wild.html>

- DRAM



Embedded DRAM in IBM Power 7+ microprocessor (32-nm)

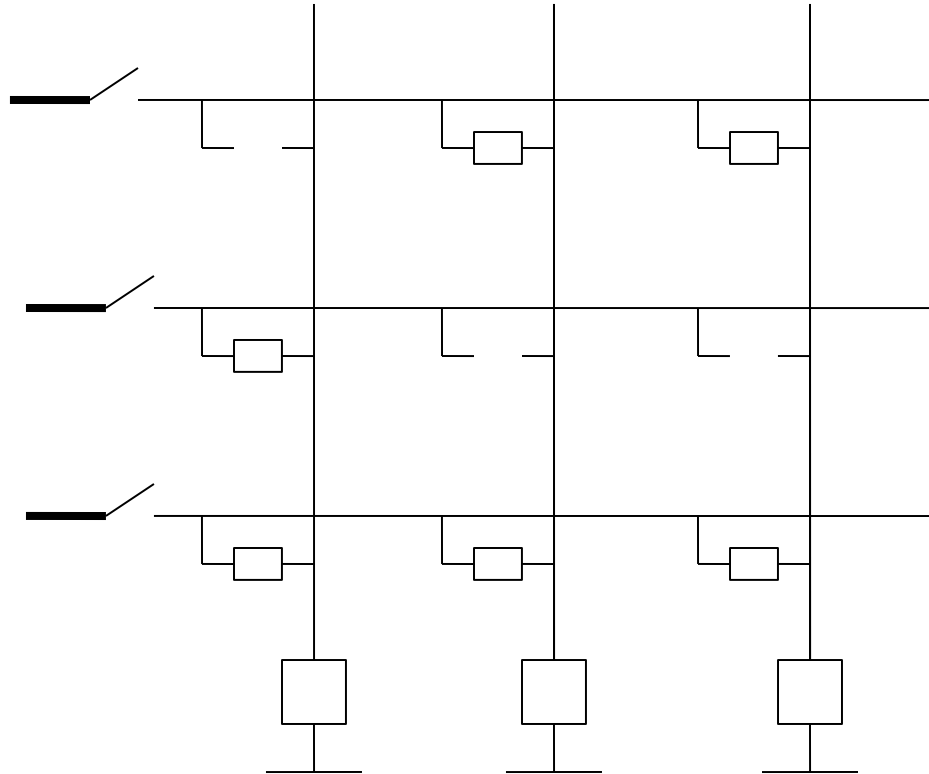
- DRAM



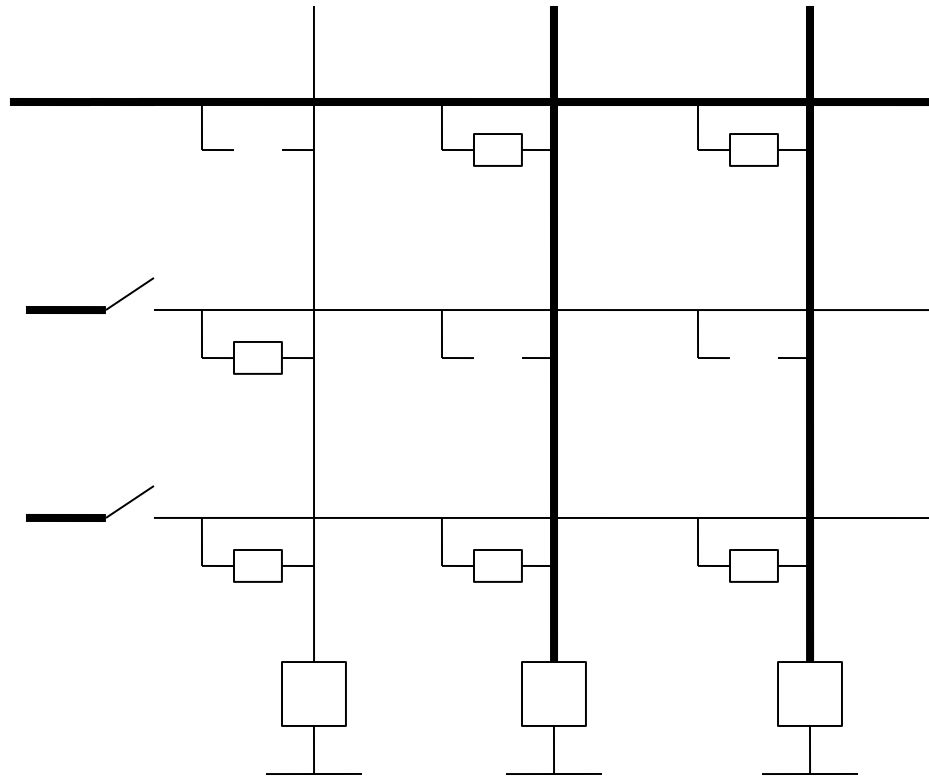
Intel's 22-nm embedded DRAM stack

Permanentspeicher (non-volatile)

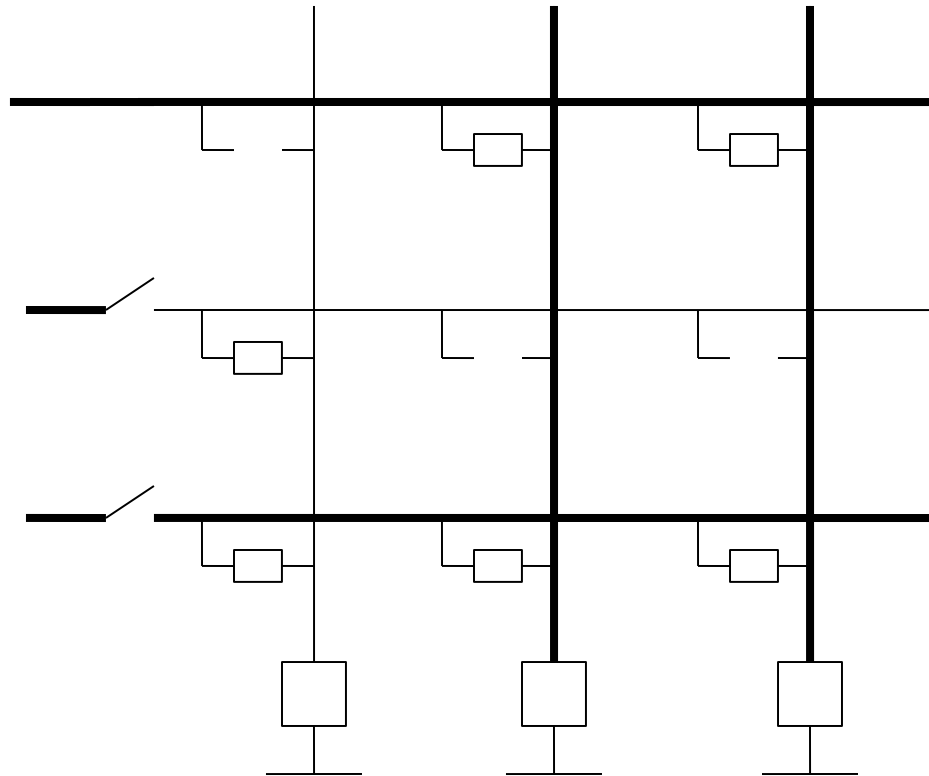
- Speicherzugriff
- Idee



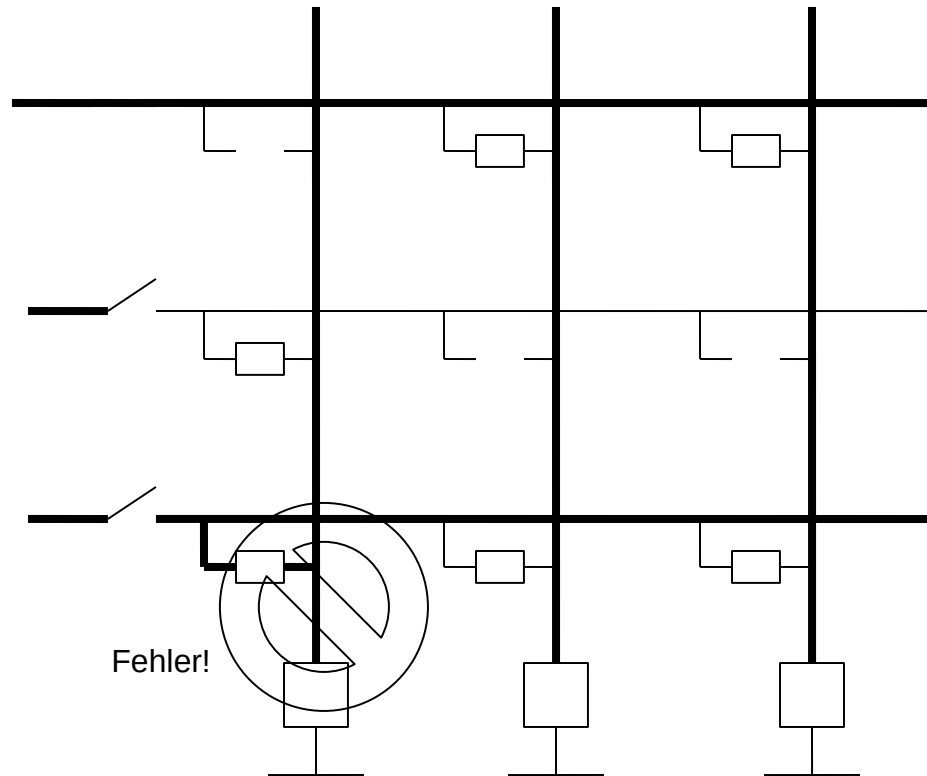
- Speicherzugriff
- Idee



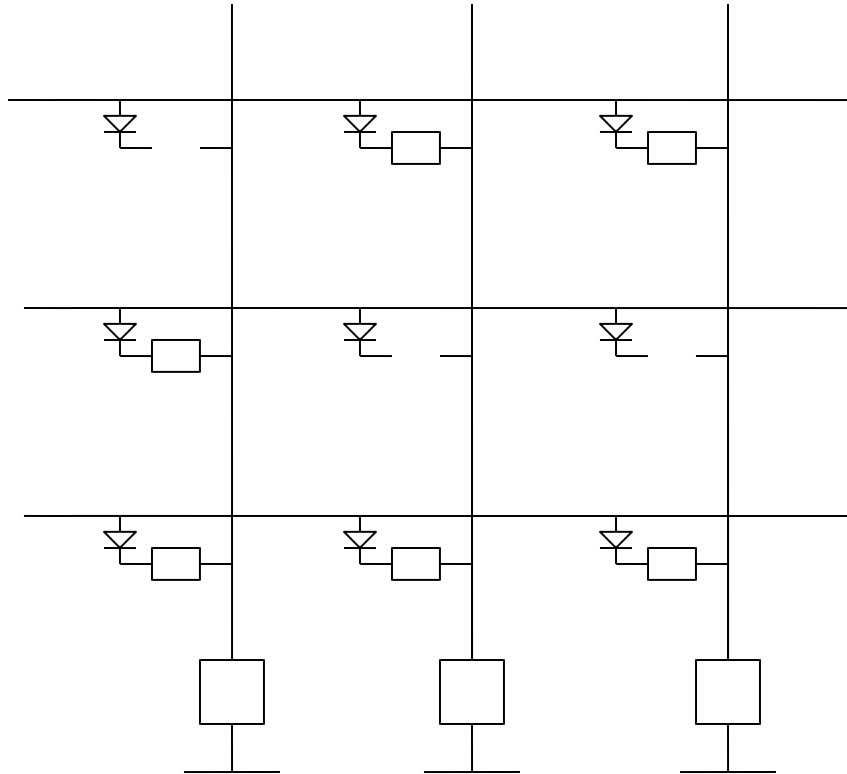
- Speicherzugriff
- Idee



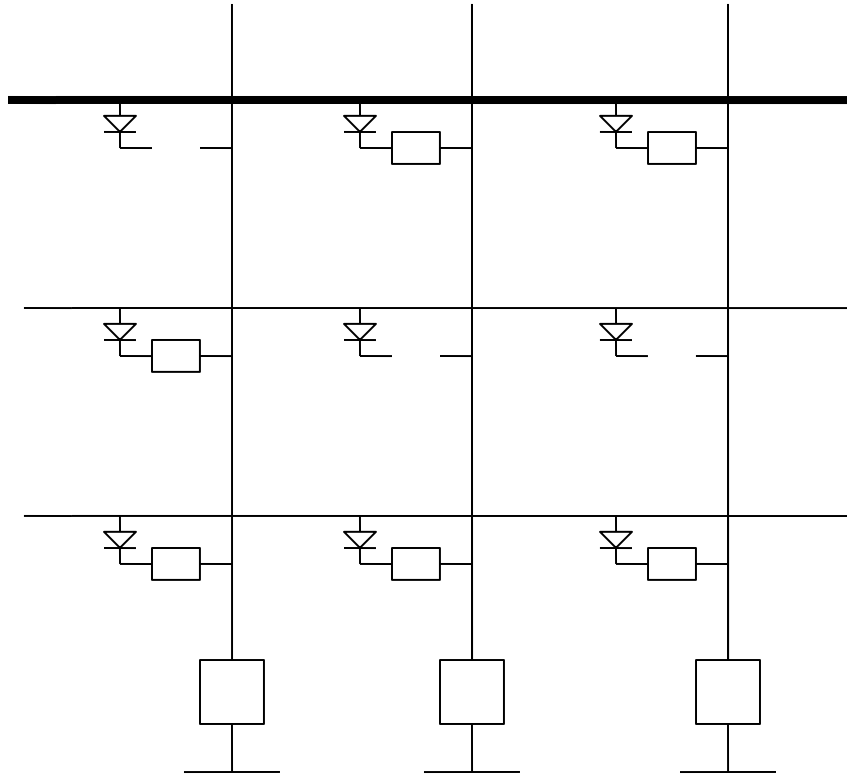
- Speicherzugriff
- Idee



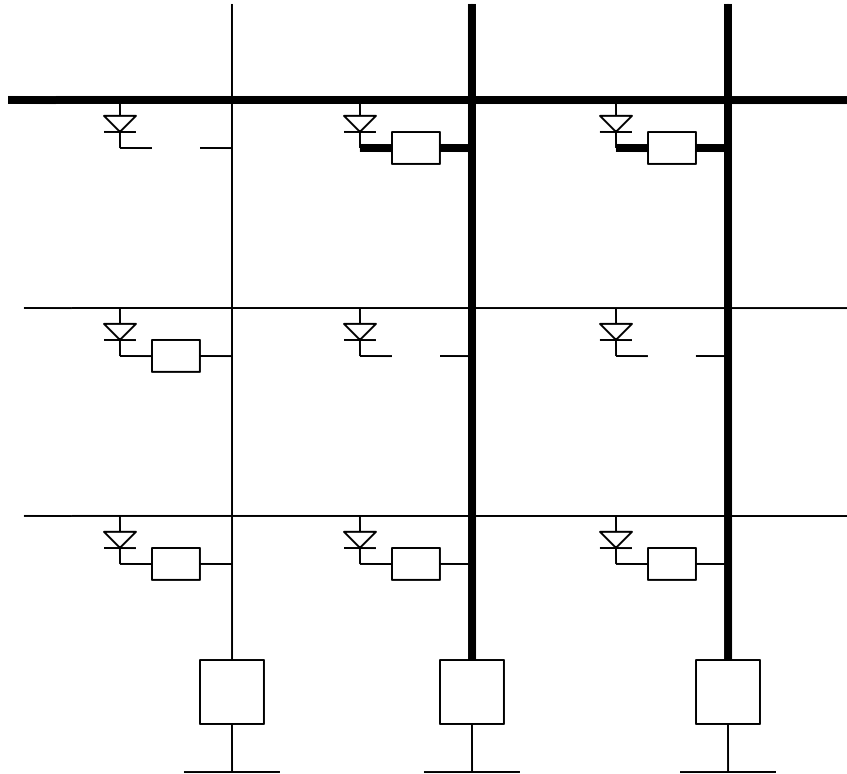
- Speicherzugriff
- Dioden



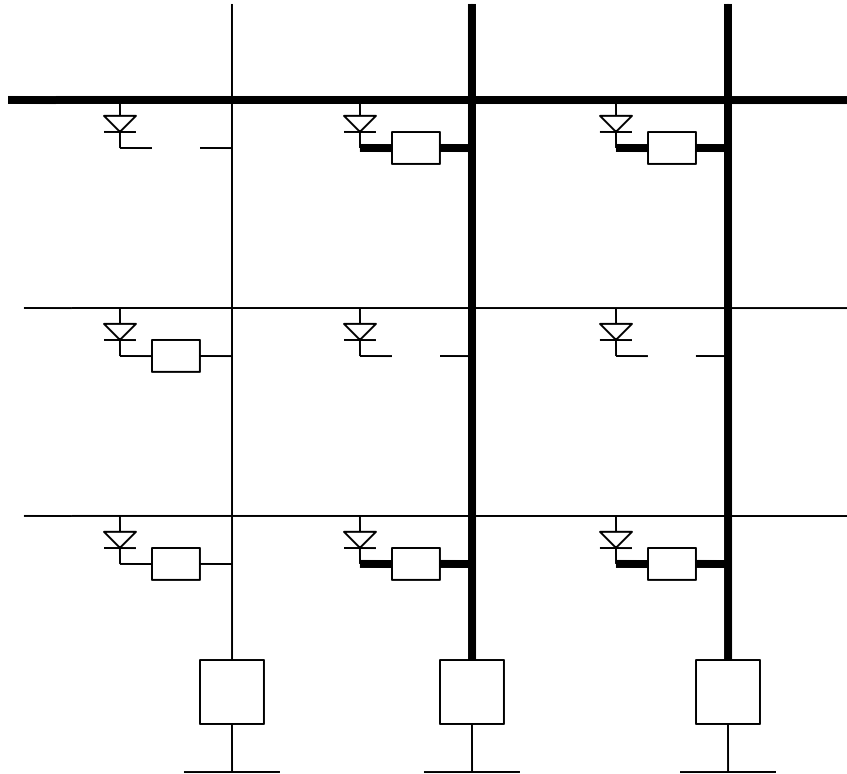
- Speicherzugriff
- Dioden



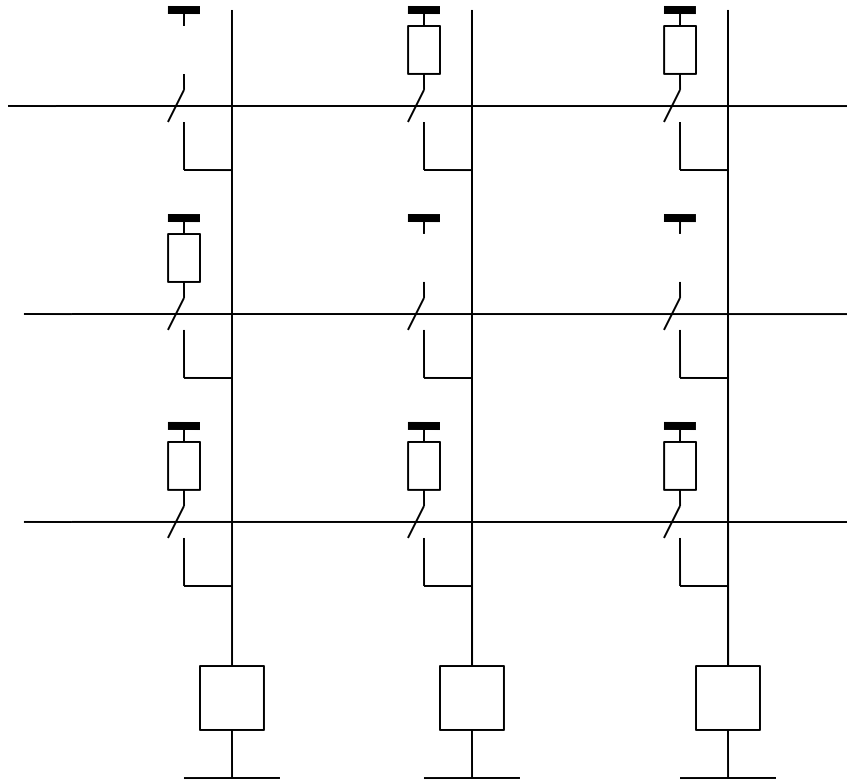
- Speicherzugriff
- Dioden



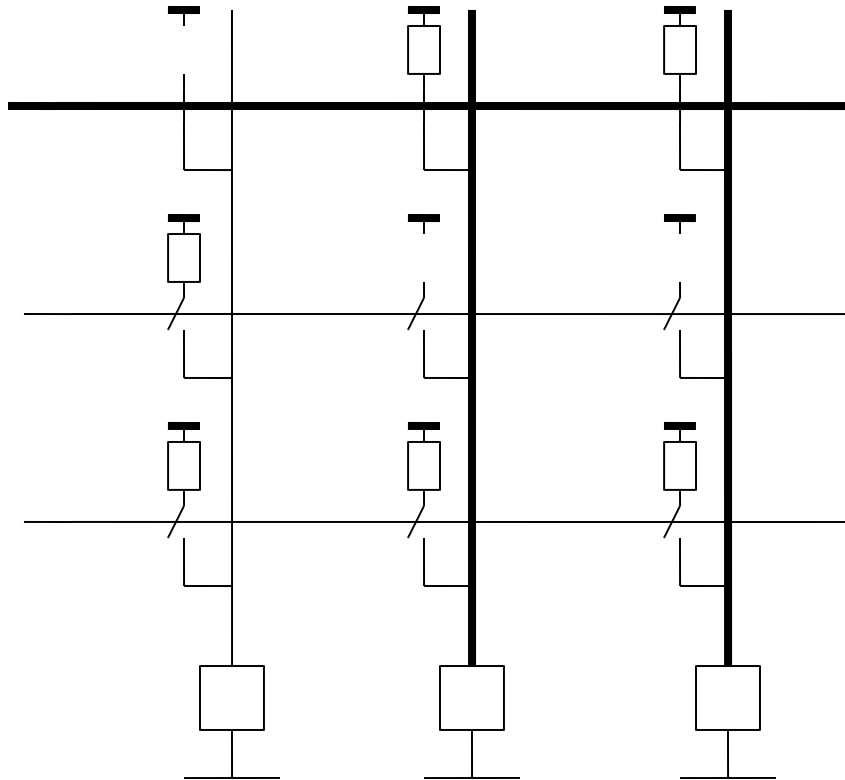
- Speicherzugriff
- Dioden



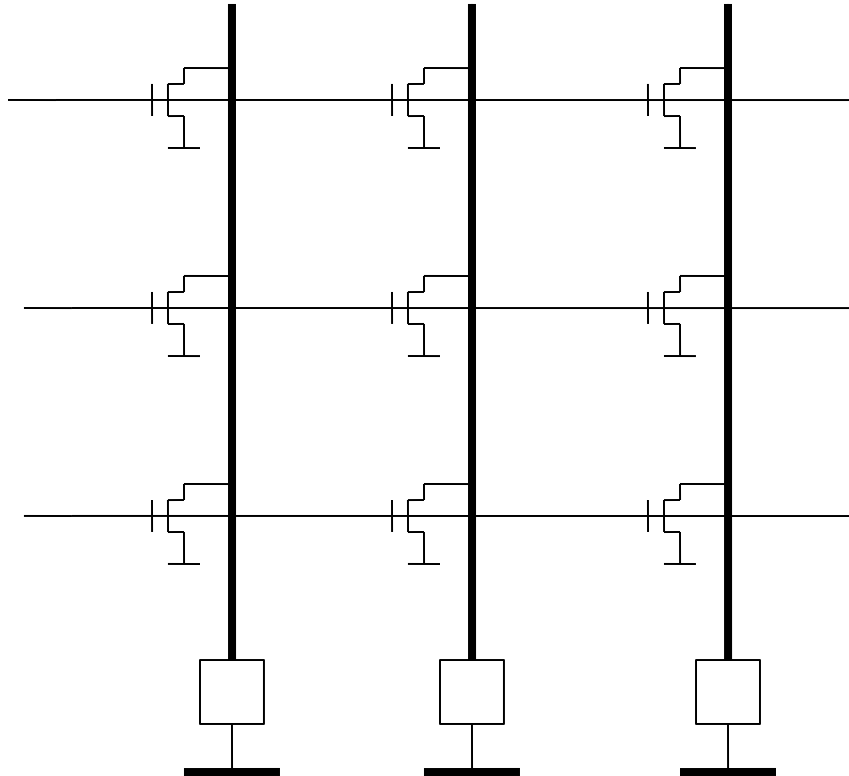
- Speicherzugriff
- Schalter



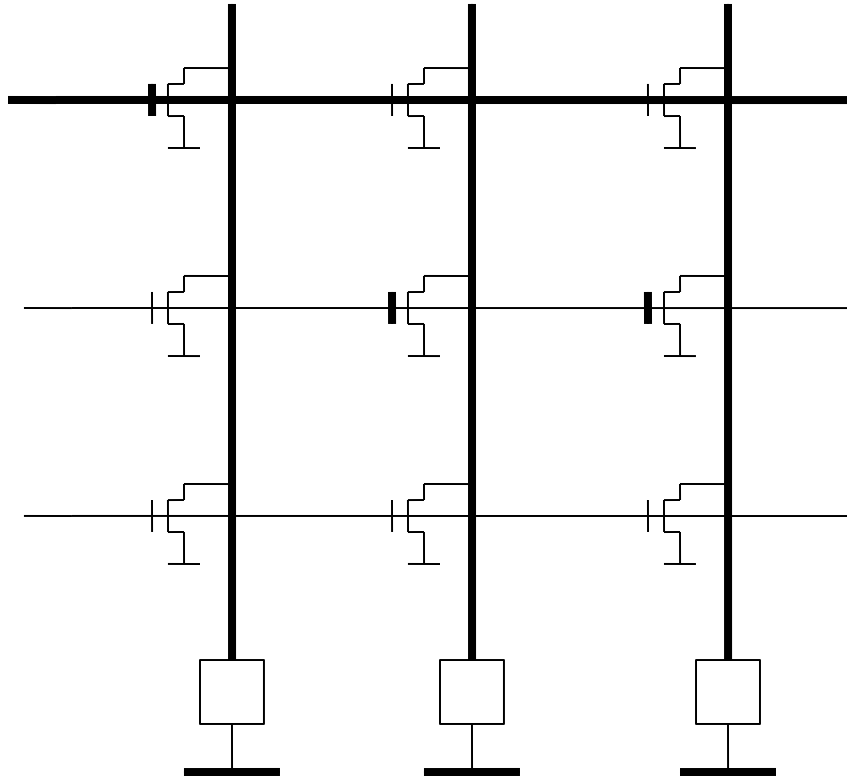
- Speicherzugriff
- Schalter



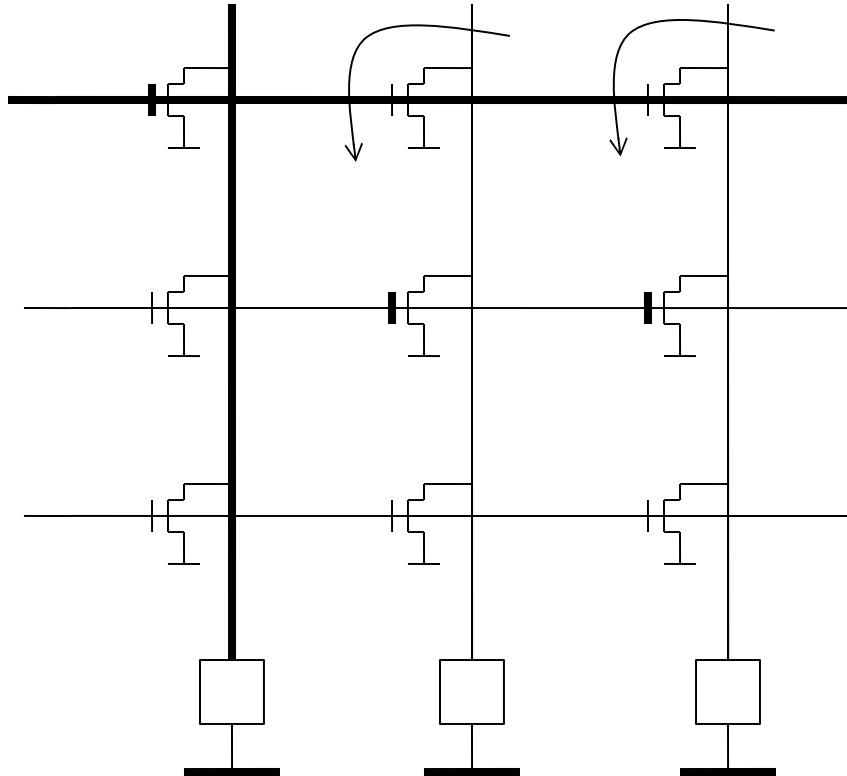
- Speicherzugriff
- Transistor (ODER-Schaltung)



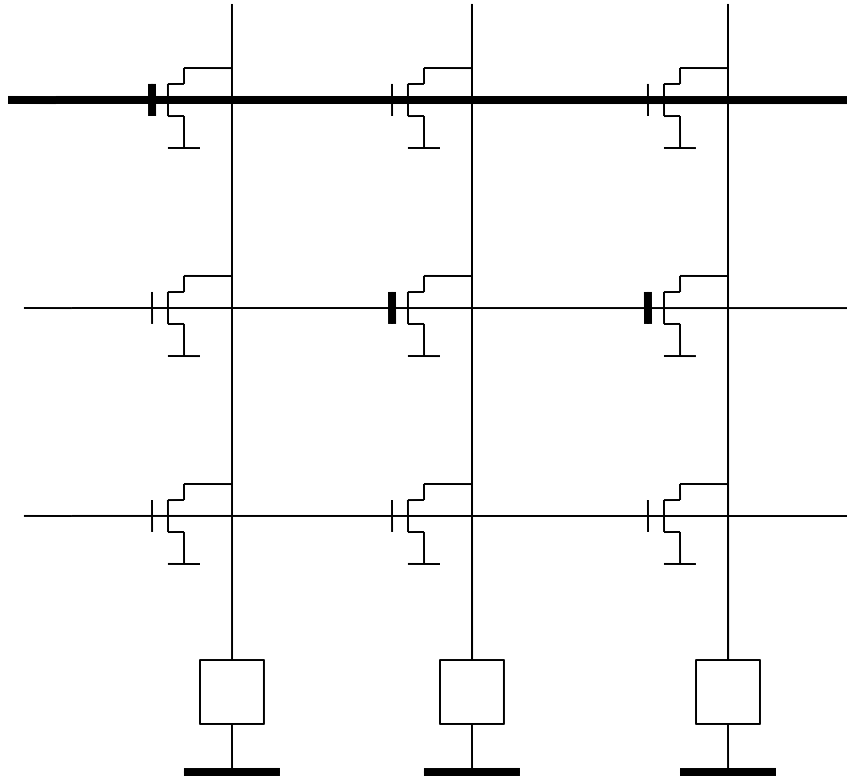
- Speicherzugriff
- Transistor (ODER-Schaltung)



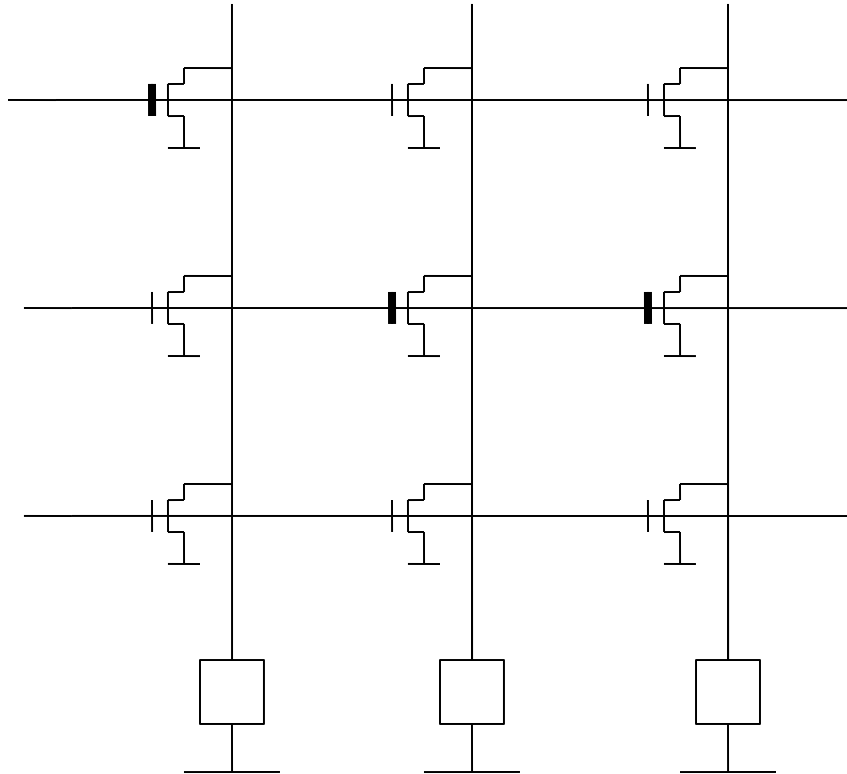
- Speicherzugriff
- Transistor (ODER-Schaltung)



- Speicherzugriff
- Transistor (ODER-Schaltung)

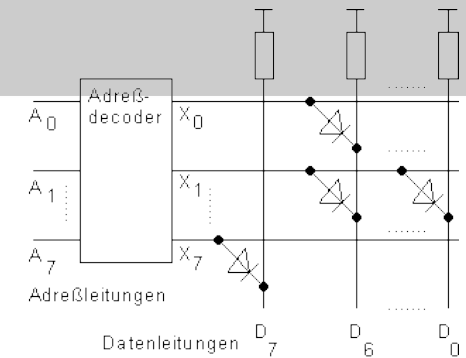
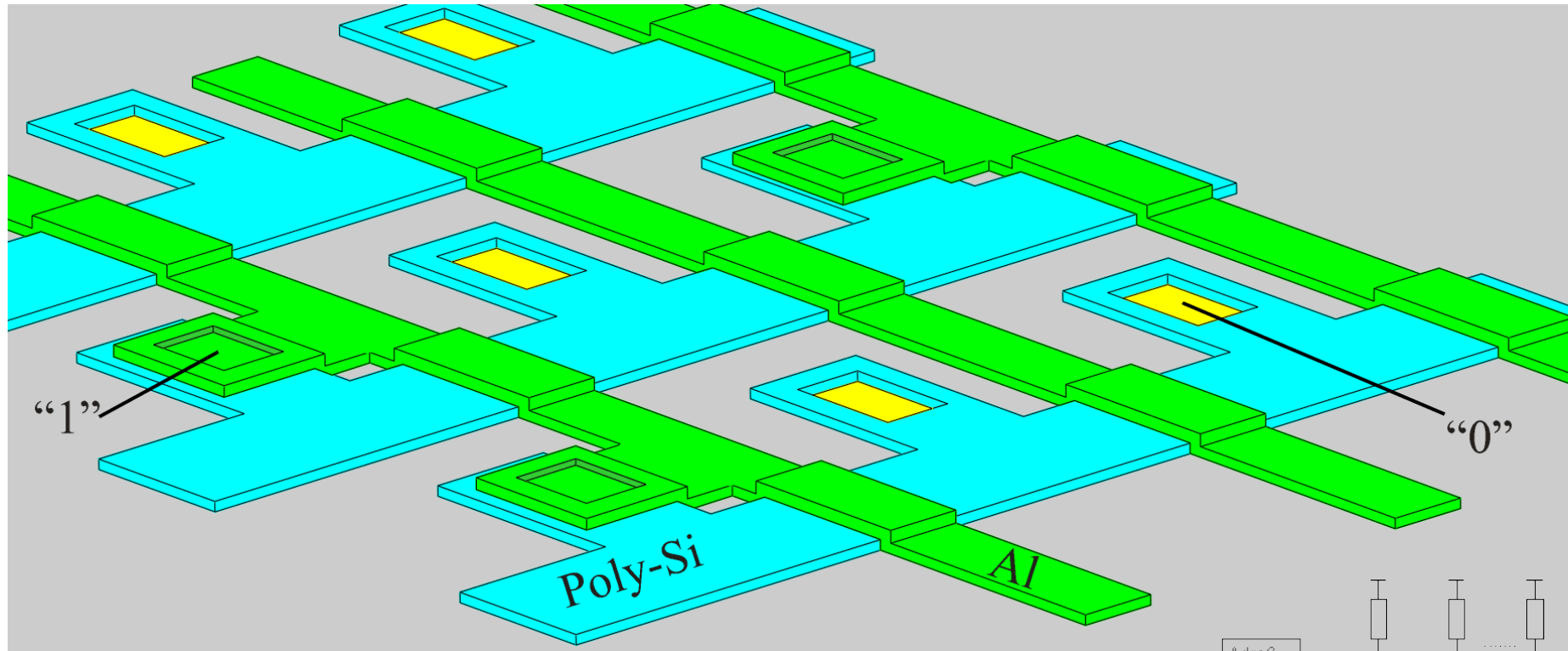


- Speicherzugriff
- Transistor (ODER-Schaltung)



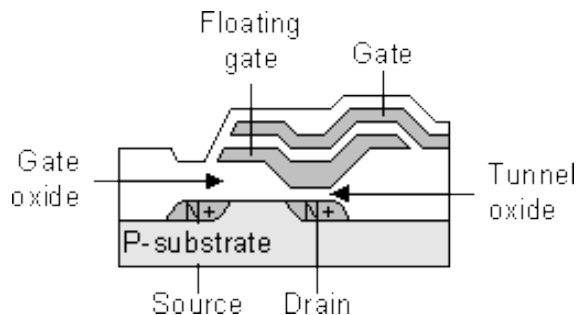
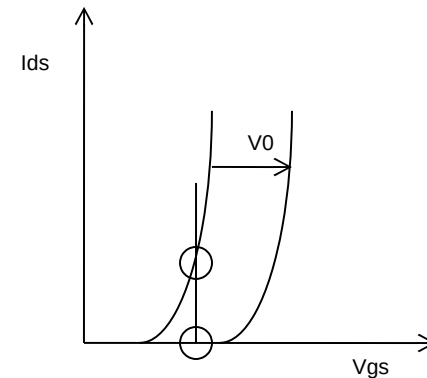
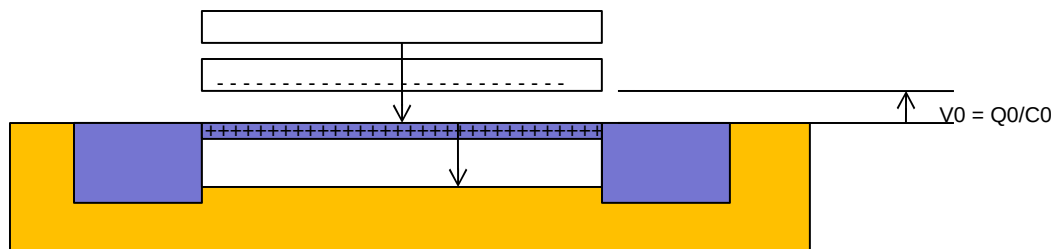
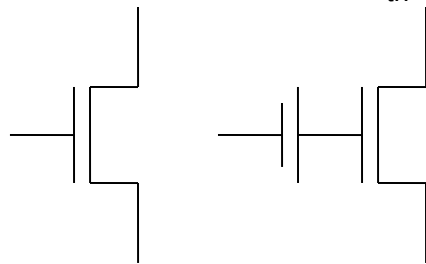
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ROM

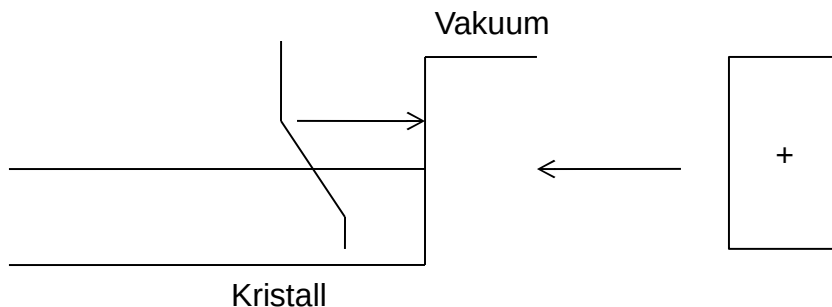


EPROM, EEPROM und FLASH

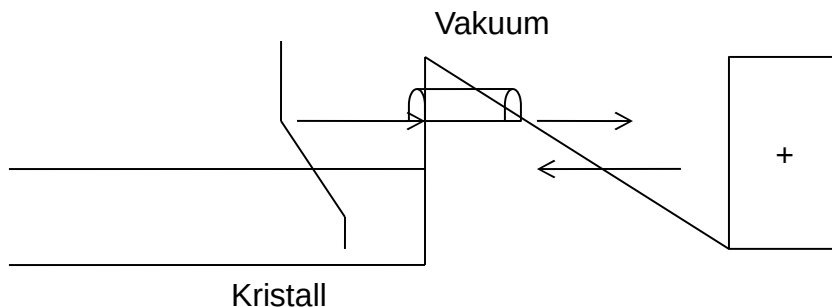
- Durch die gespeicherte Ladung wird die Schwellspannung des Transistors zu höheren Werten verschoben. Das Auslesen erfolgt bei niedrigen Spannungen. Ist U_{th} verschoben, schaltet der Transistor nicht ein.



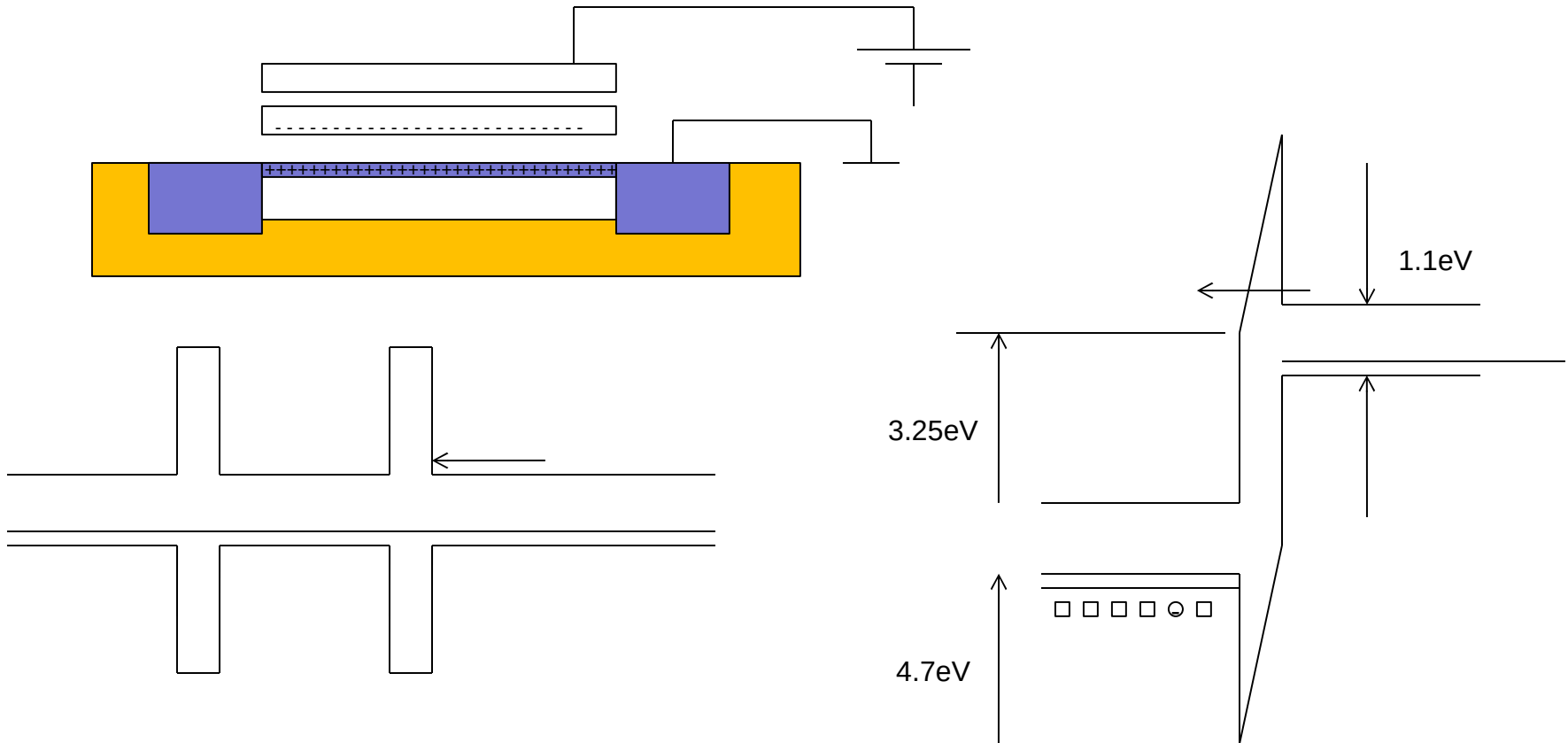
- Bei der **Feldemission** werden durch ein ausreichend starkes elektrisches Feld (mehr als 10^9 V/m) Elektronen mit einer sehr geringen Energiebreite aus einer (negativ geladenen) Kathode gelöst. Klassisch betrachtet ist es für ein Teilchen mit einer bestimmten mittleren thermischen Energie, die kleiner ist als die Höhe der Austrittsarbeit, unmöglich, das Kathodenmaterial zu verlassen. Quantenmechanisch betrachtet gibt es jedoch eine bestimmte Wahrscheinlichkeit, dass einzelne Elektronen aus dem Festkörper austreten. Diese werden dann durch das hohe äußere Feld abgesaugt. Diesen Effekt nennt man allgemein auch Tunneleffekt. Das Elektron tunnelt also durch den Potentialwall, der durch das äußere elektrische Feld verkippt wurde – diese spezielle Art von Tunneln nennt man auch „**Fowler-Nordheim-Tunneln**“ (benannt nach Ralph Howard Fowler und Lothar Nordheim).^[1]



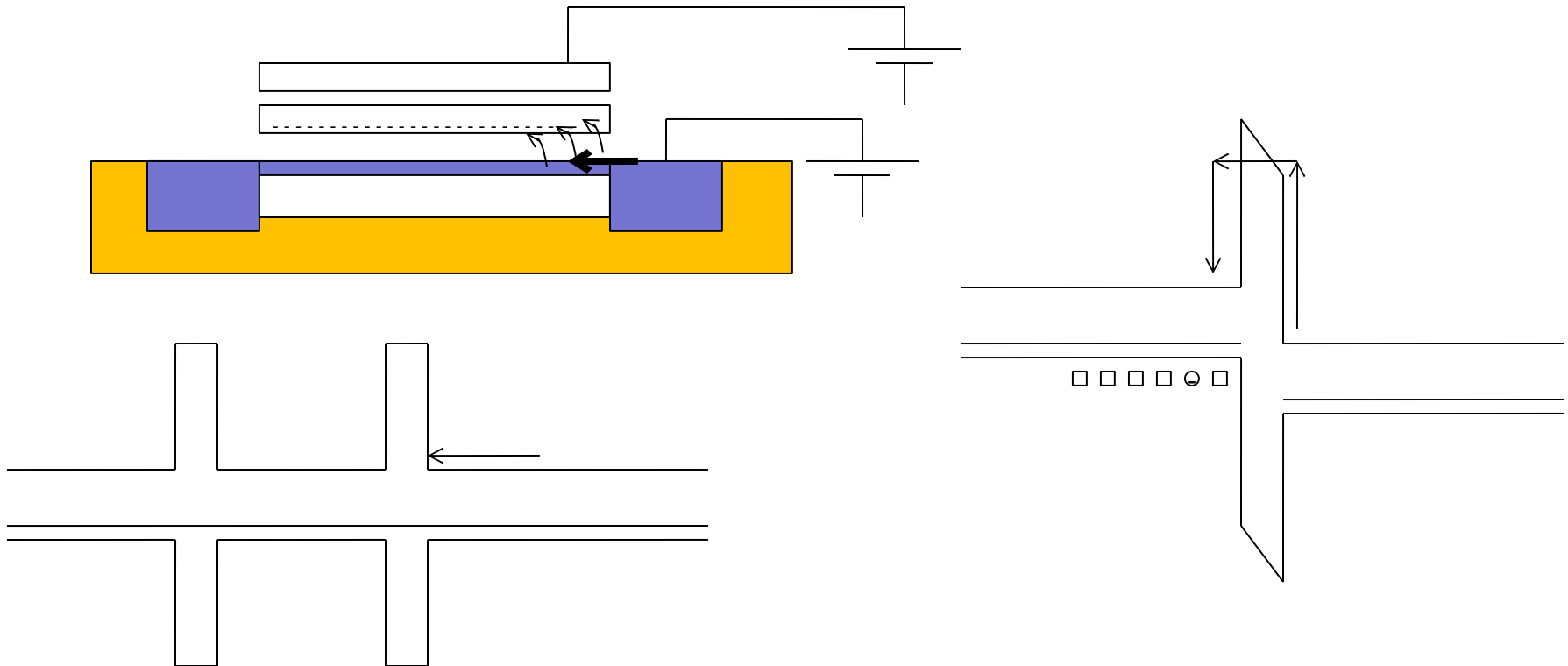
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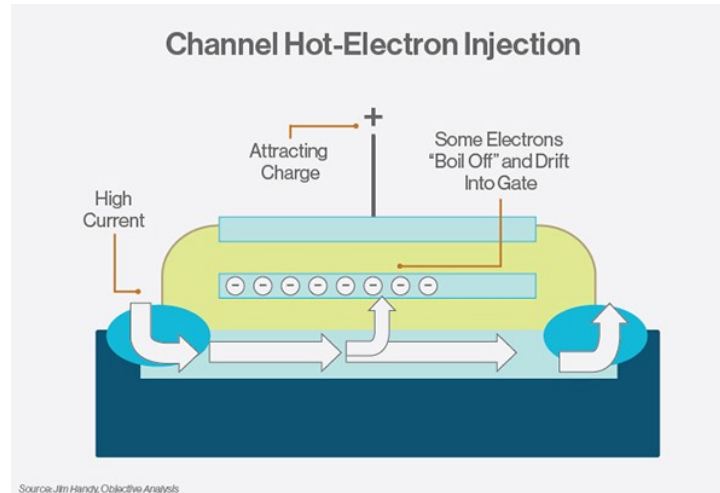
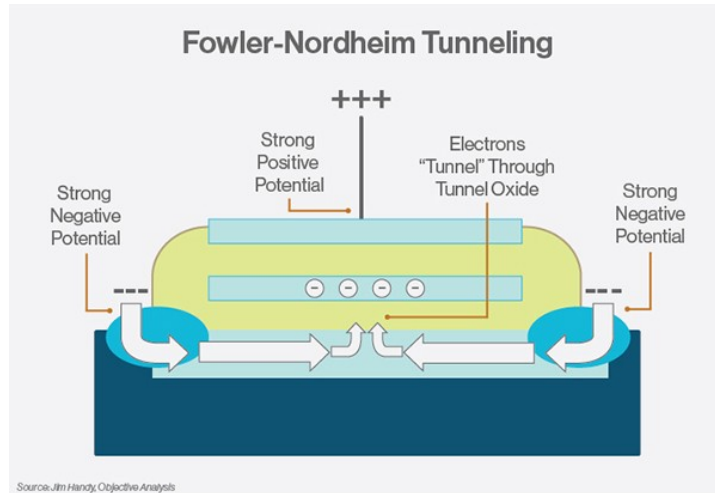
- EPROM program, Fowler-Nordheim tunnelling



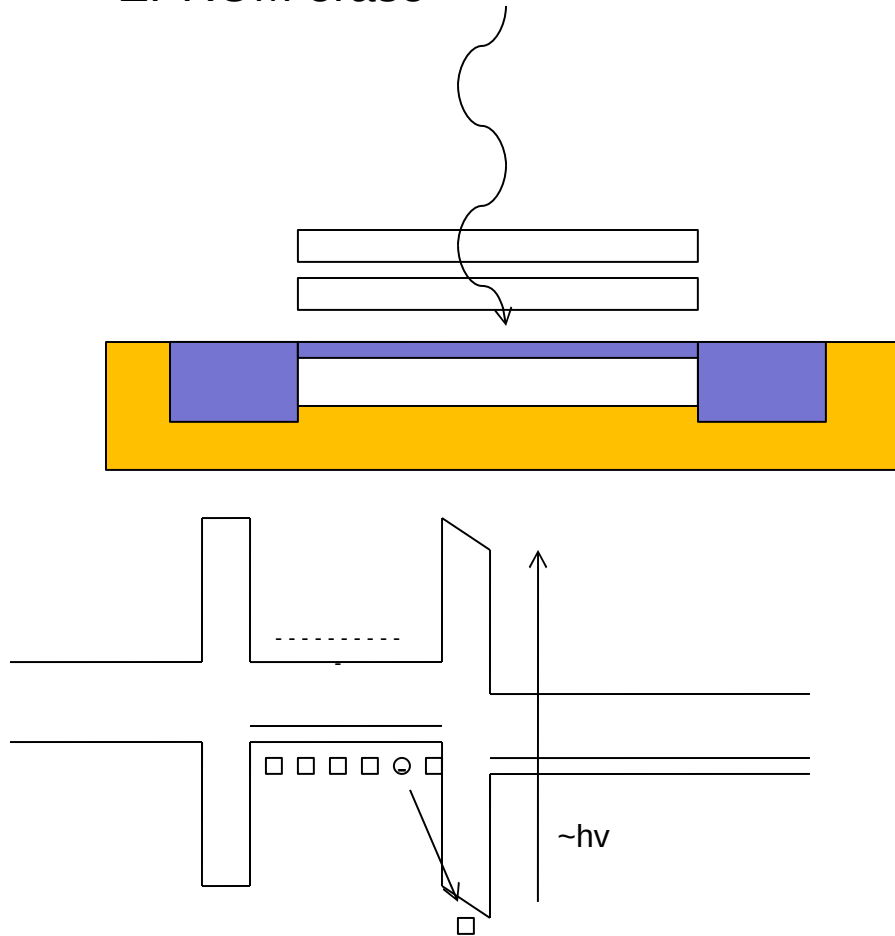
- EPROM program, channel hot carrier injection



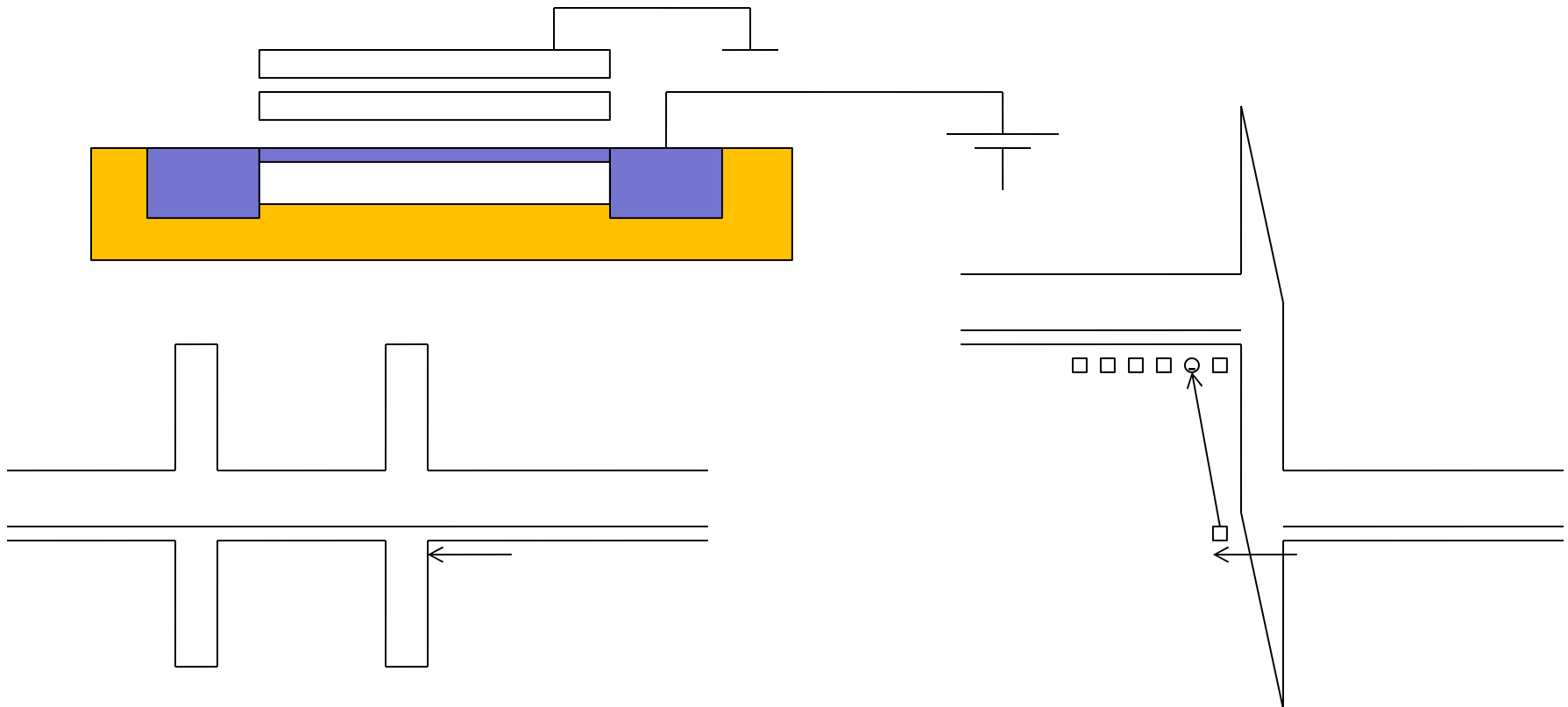
- EPROM program



- EPROM erase



- EEPROM erase, Fowler-Nordheim tunnelling

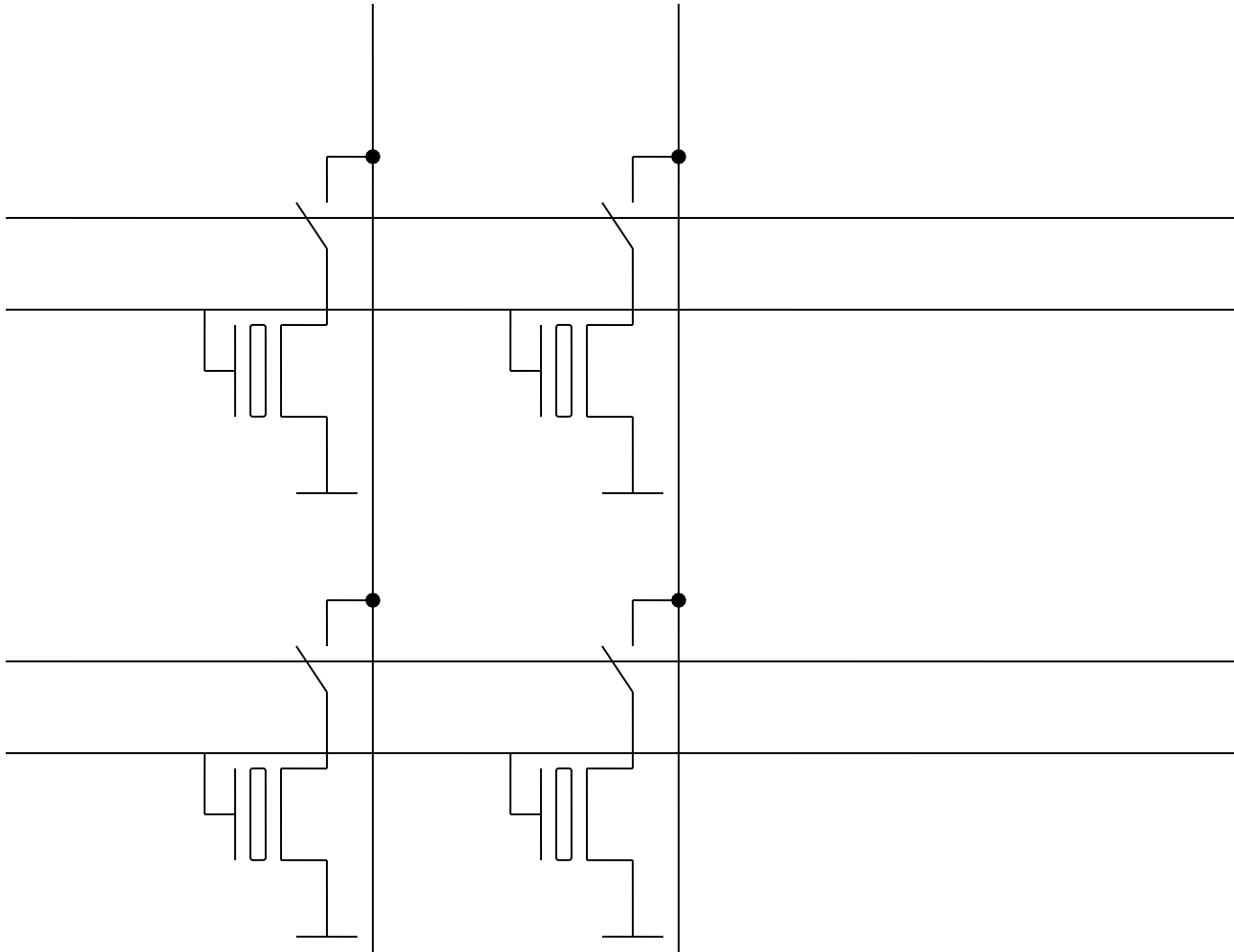


EEPROM – verschiedene Möglichkeiten

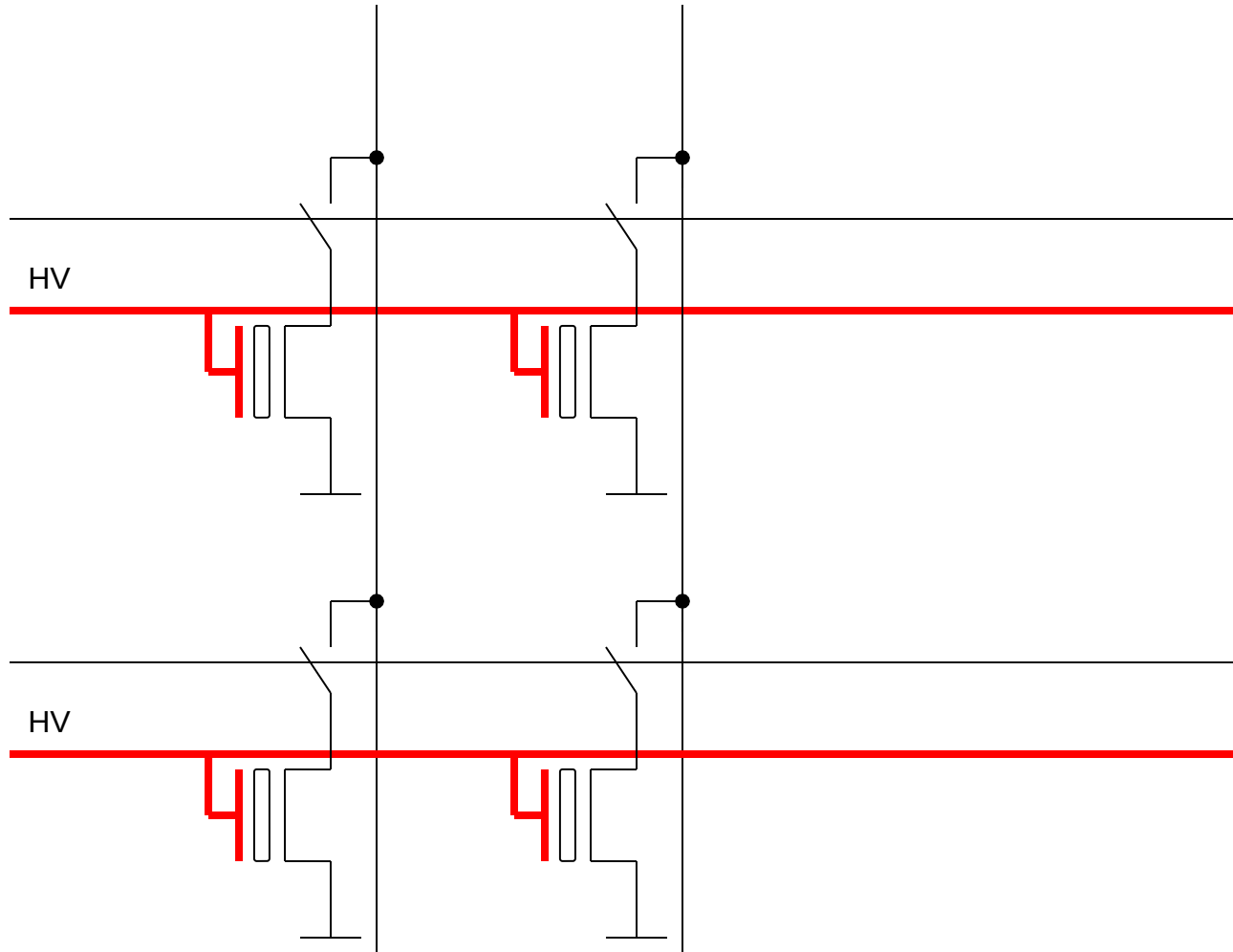
Variante 1

Erase and program based on tunnel effect

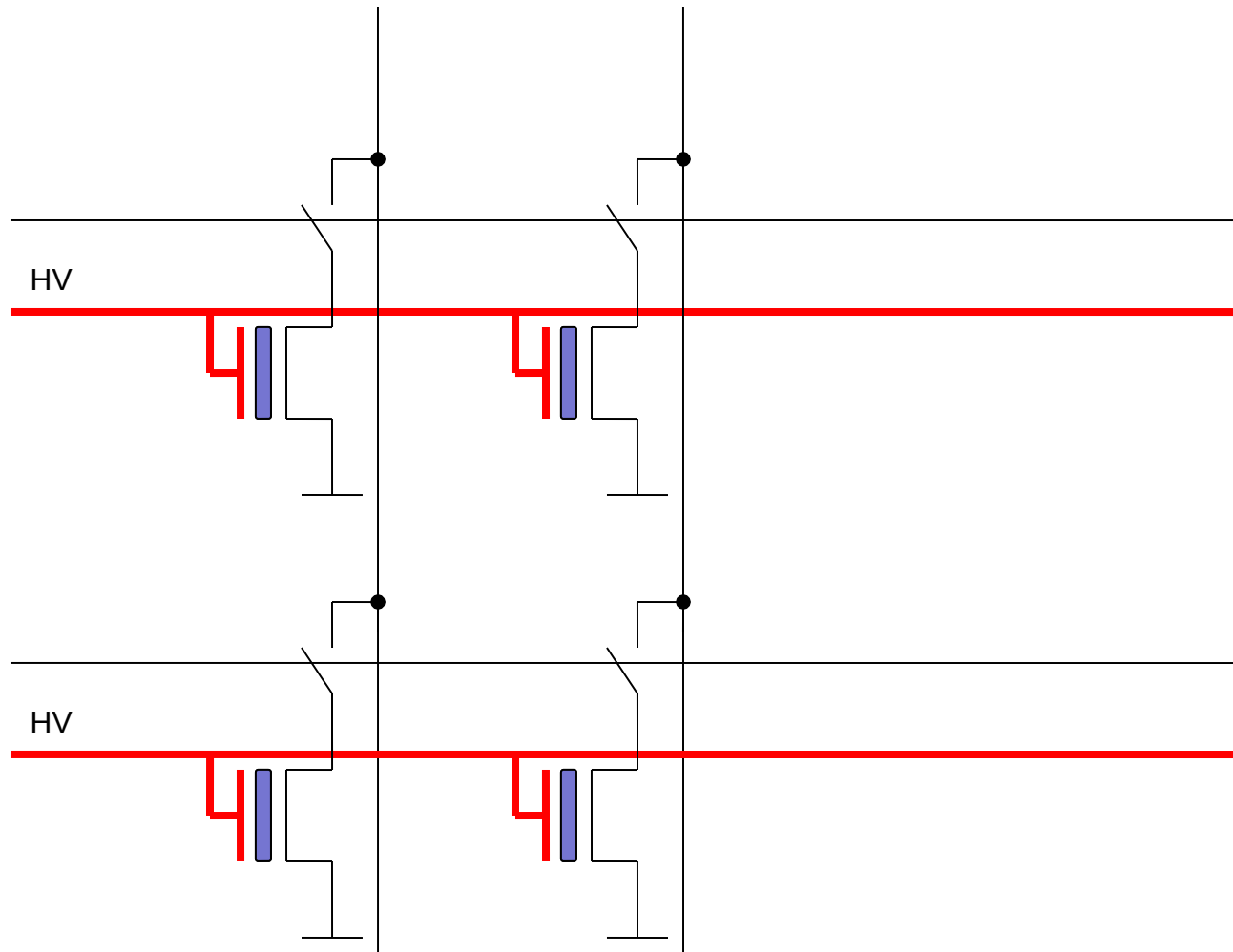
- EEPROM (erase and program based on tunnel effect)



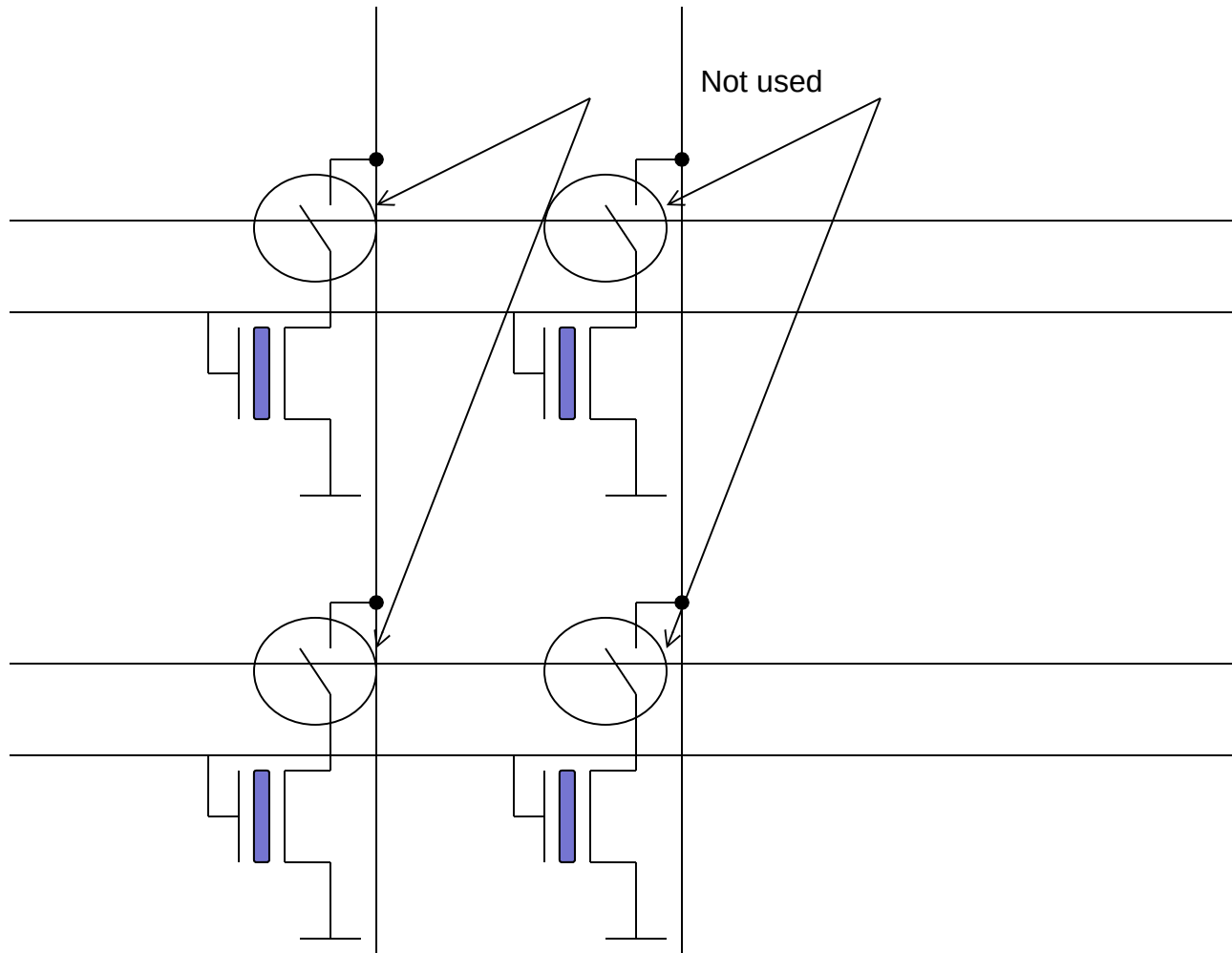
- EEPROM (erase and program based on tunnel effect)



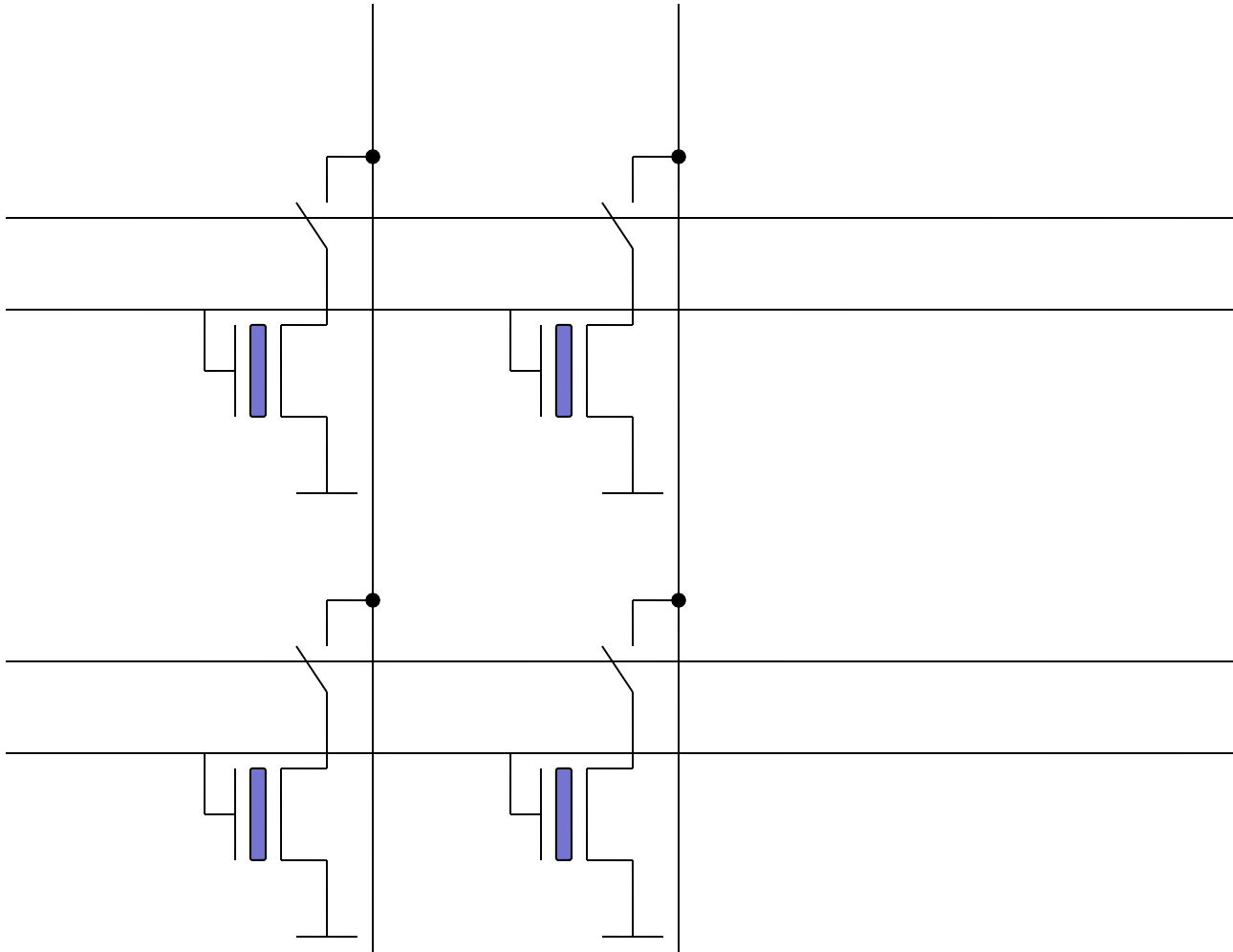
- EEPROM (erase and program based on tunnel effect)



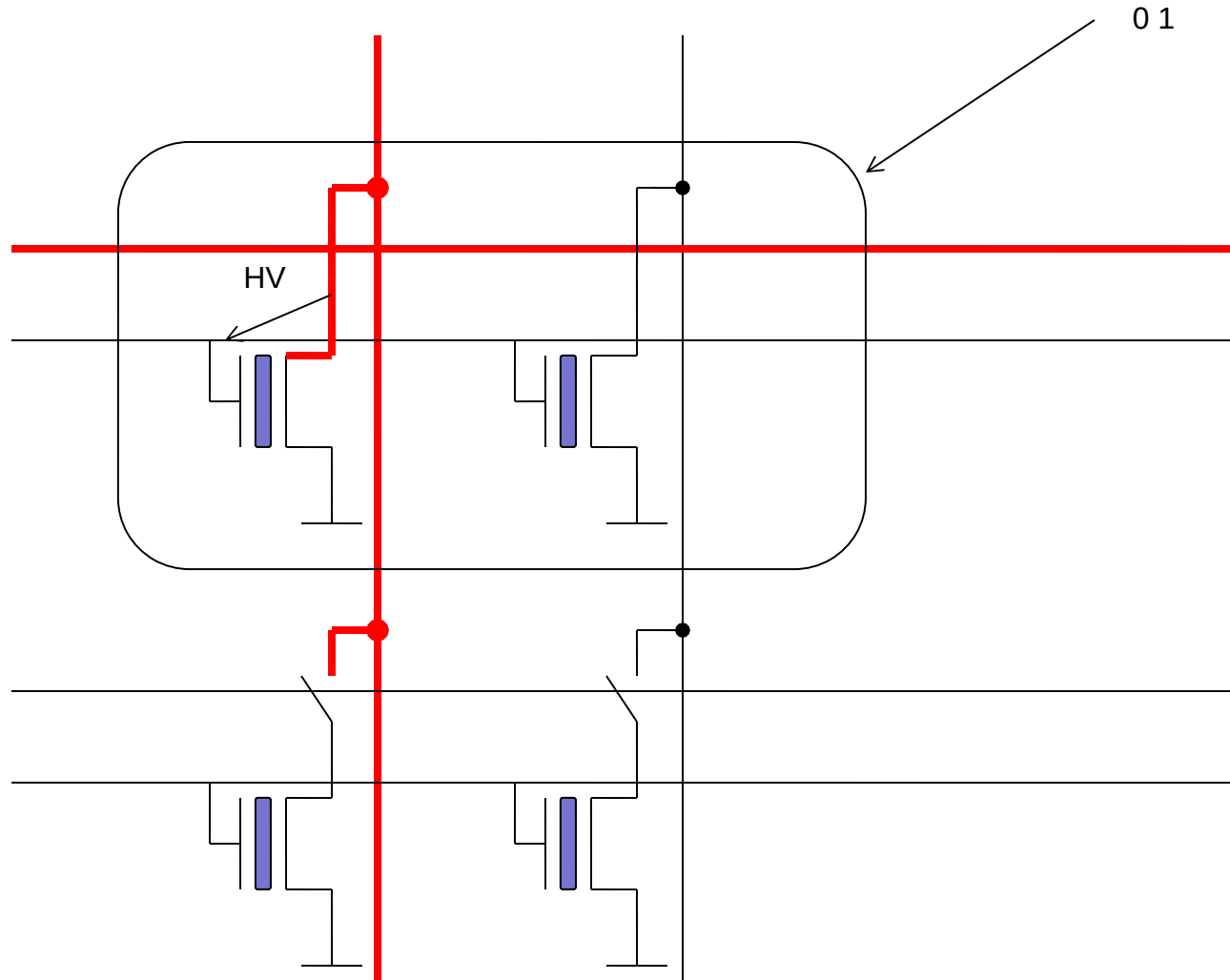
- EEPROM (erase and program based on tunnel effect)



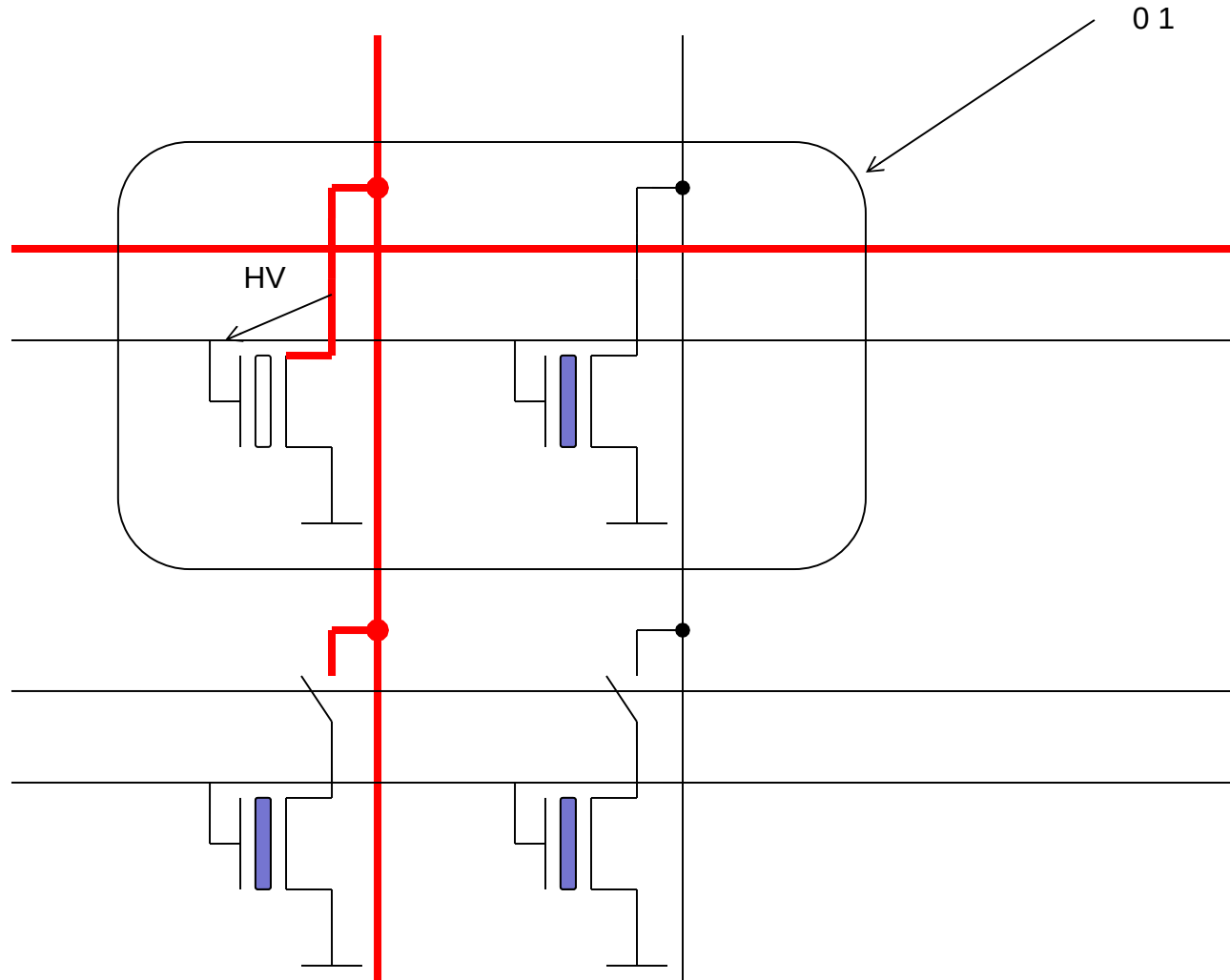
- EEPROM (erase and program based on tunnel effect)



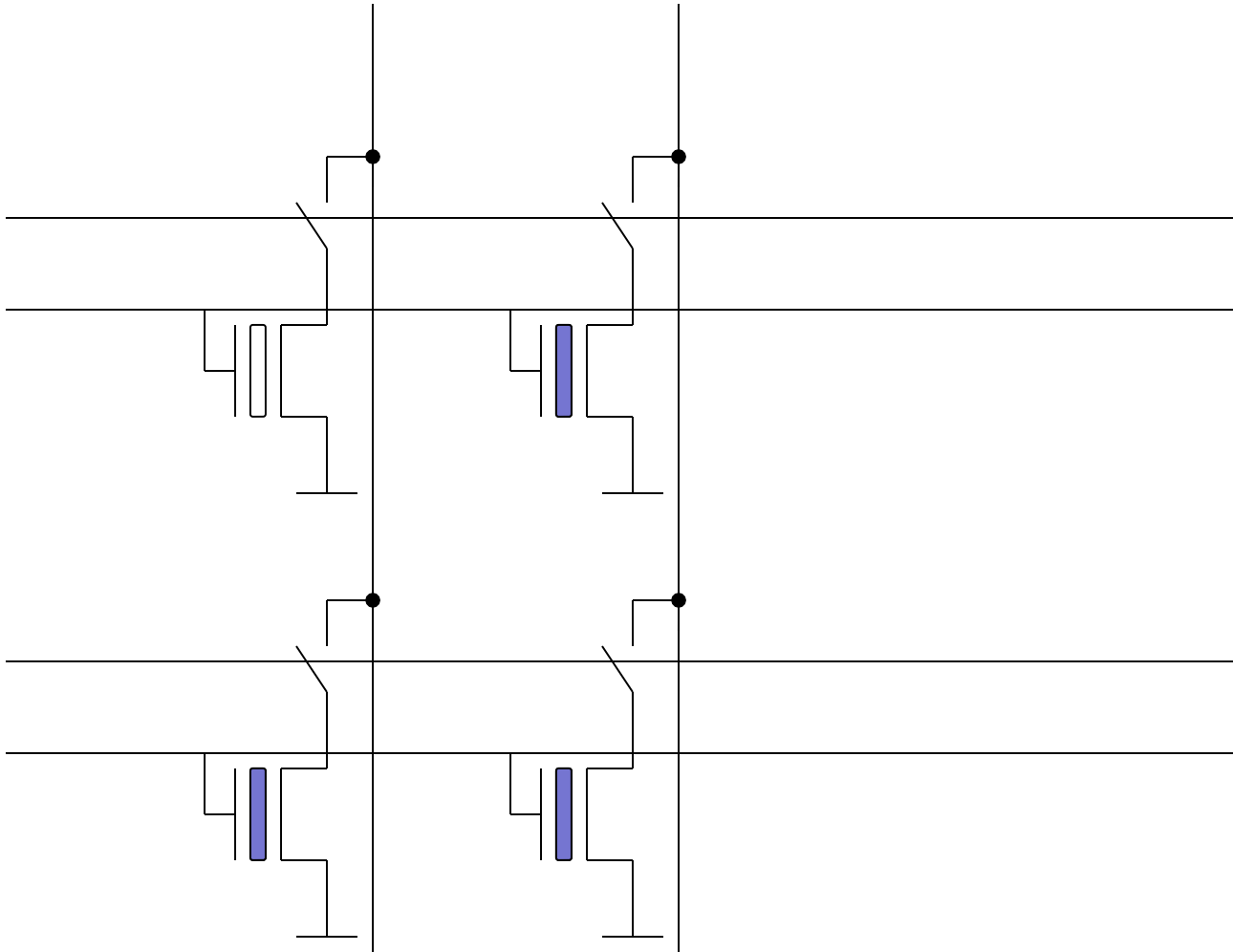
- EEPROM (erase and program based on tunnel effect)



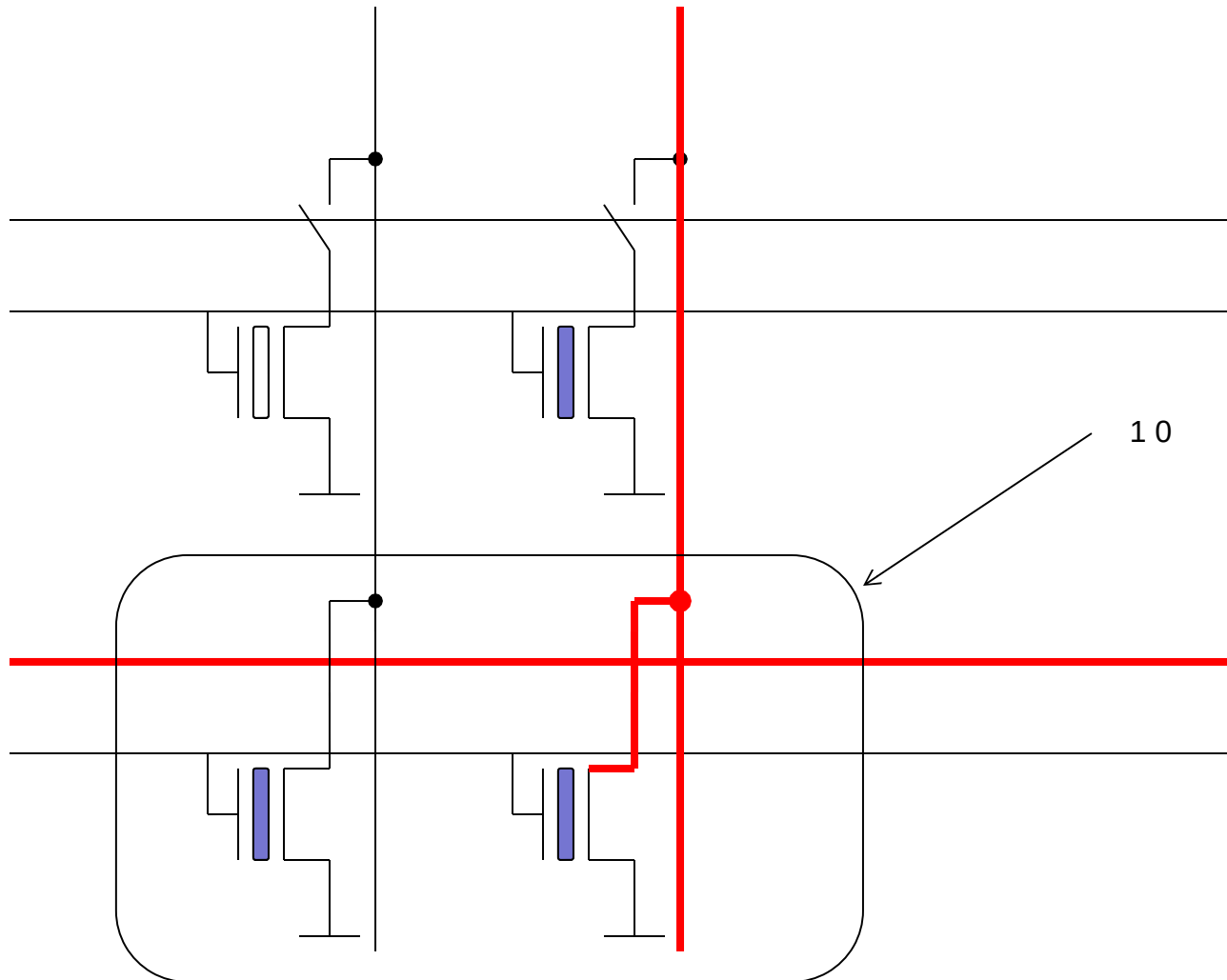
- EEPROM (erase and program based on tunnel effect)



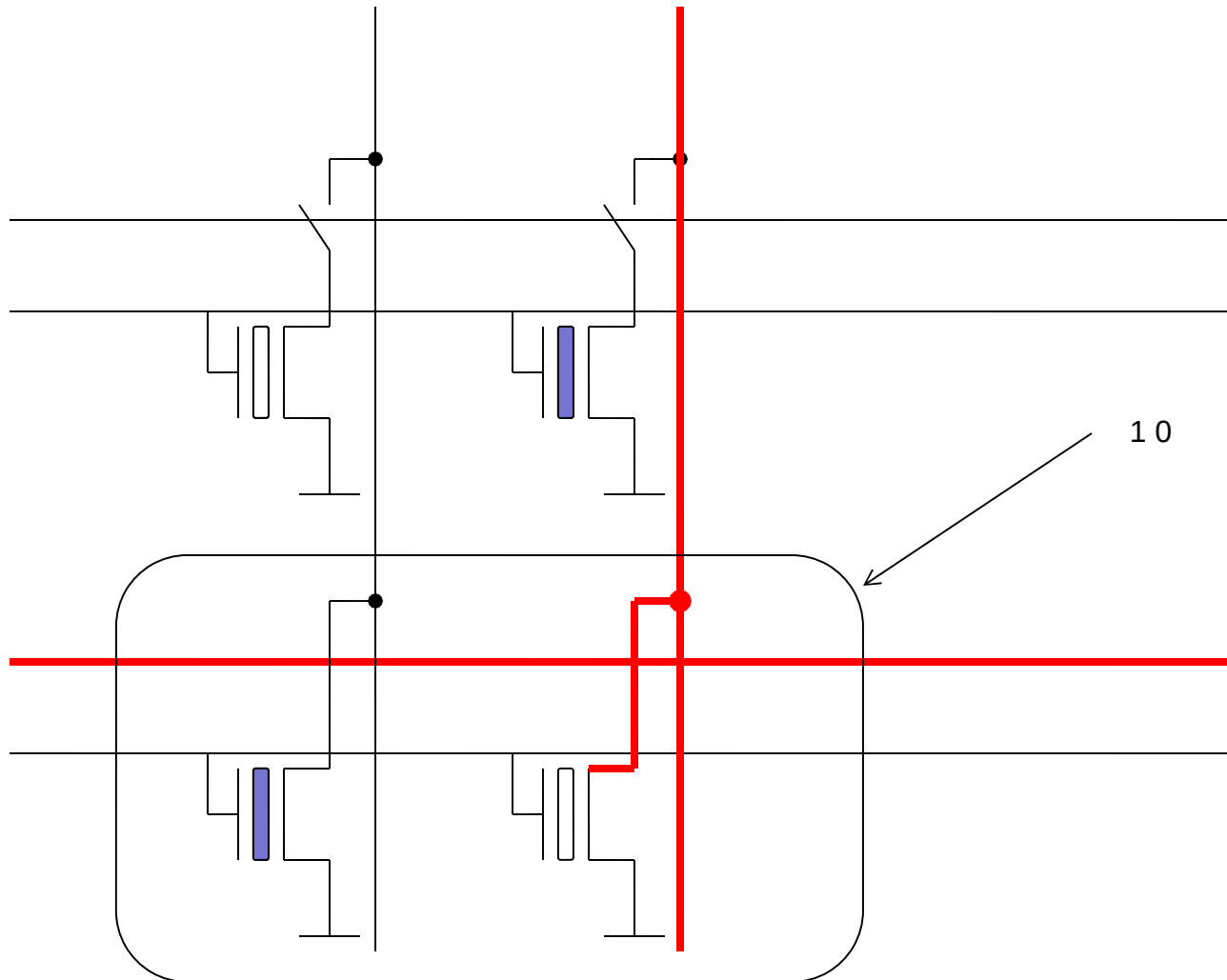
- EEPROM (erase and program based on tunnel effect)



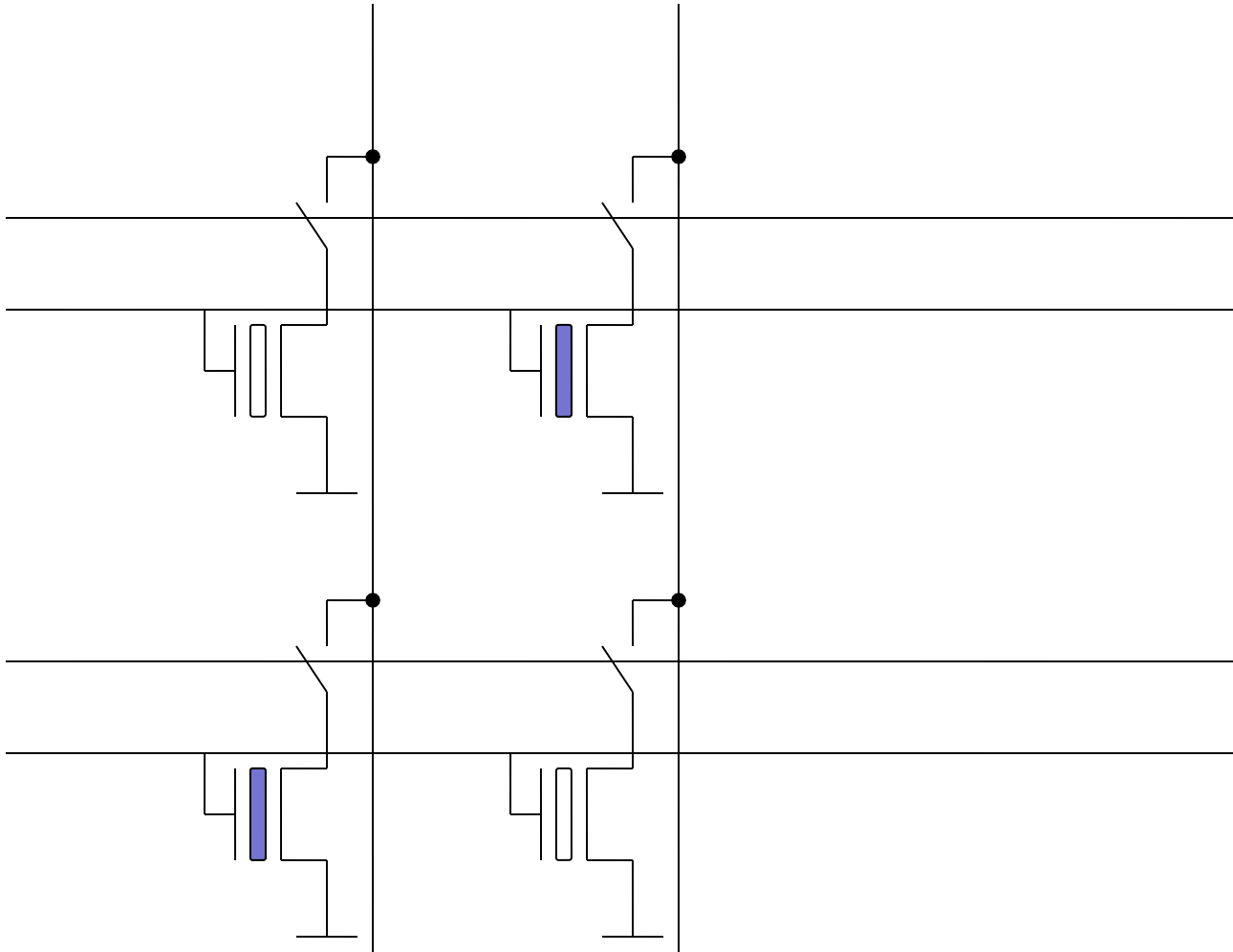
- EEPROM (erase and program based on tunnel effect)



- EEPROM (erase and program based on tunnel effect)



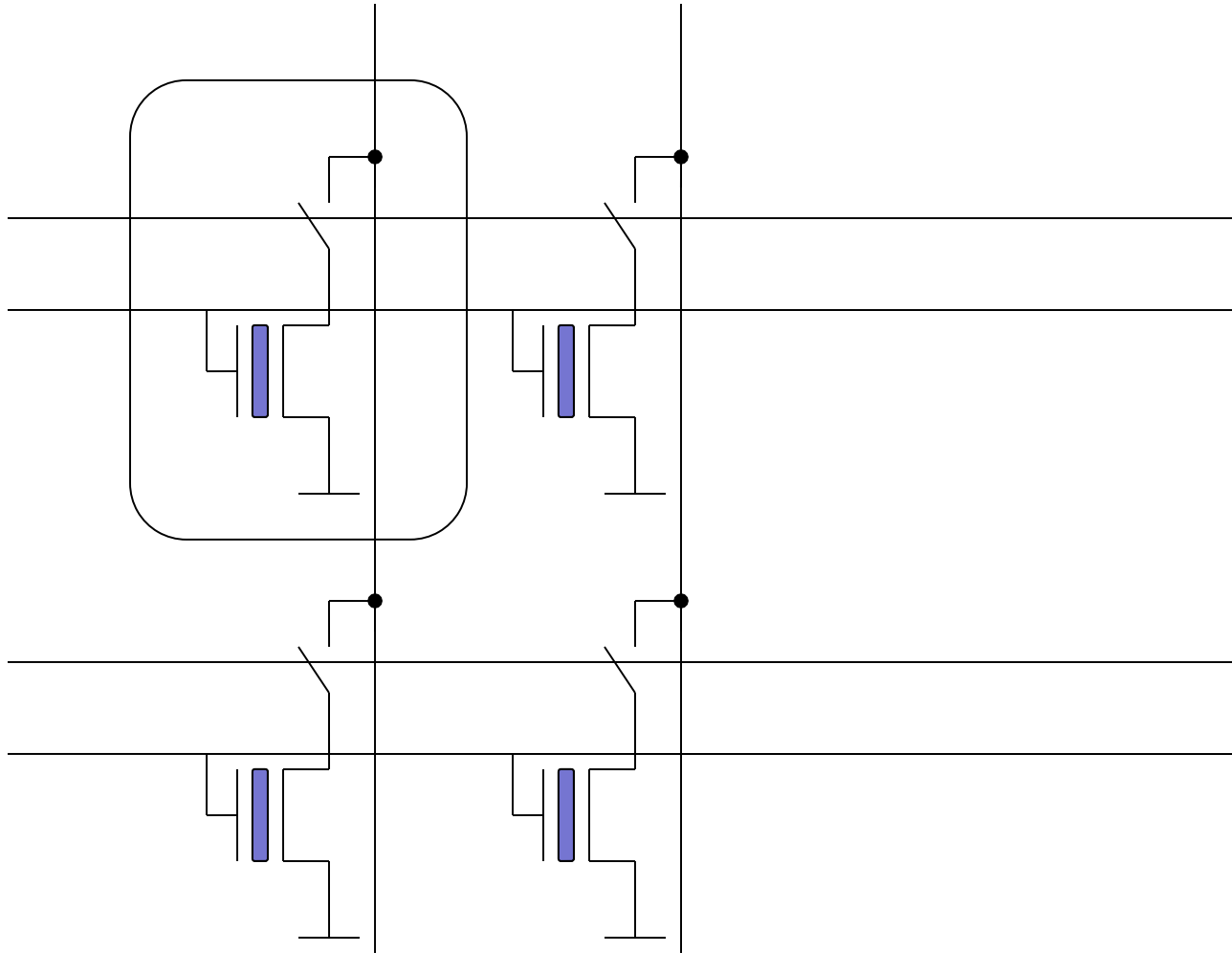
- EEPROM (erase and program based on tunnel effect)



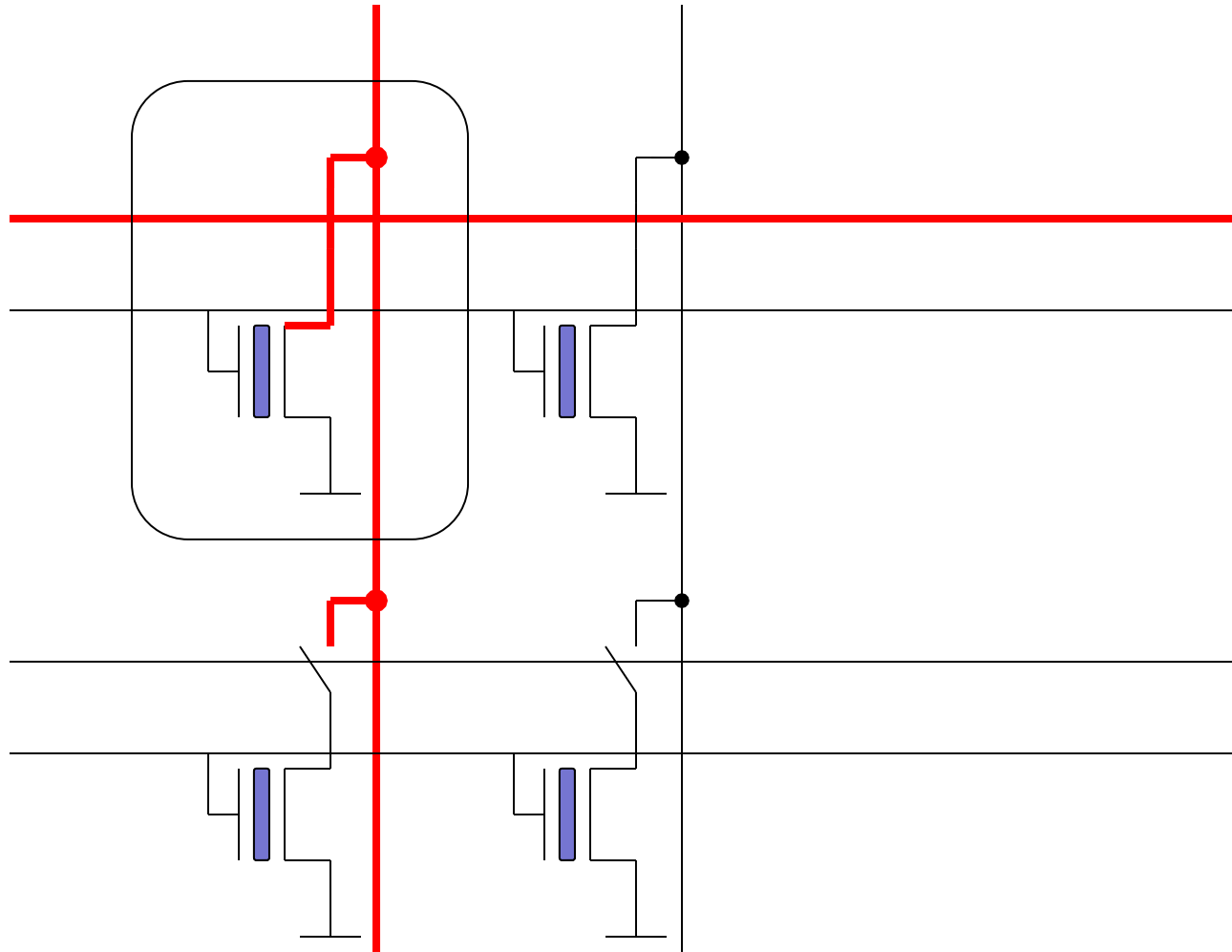
Variante 2

Erase based on tunnel effect, program based on hot carriers injection

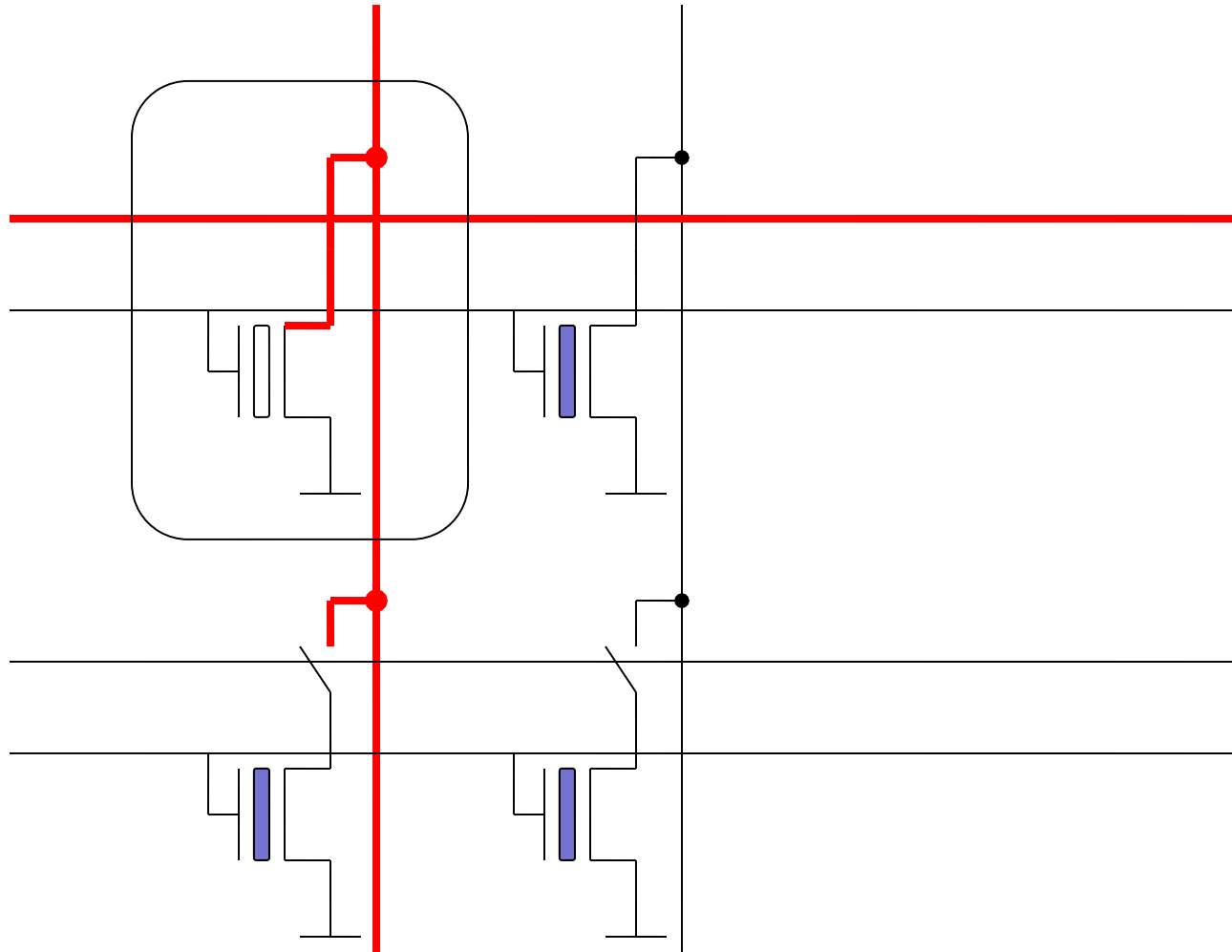
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



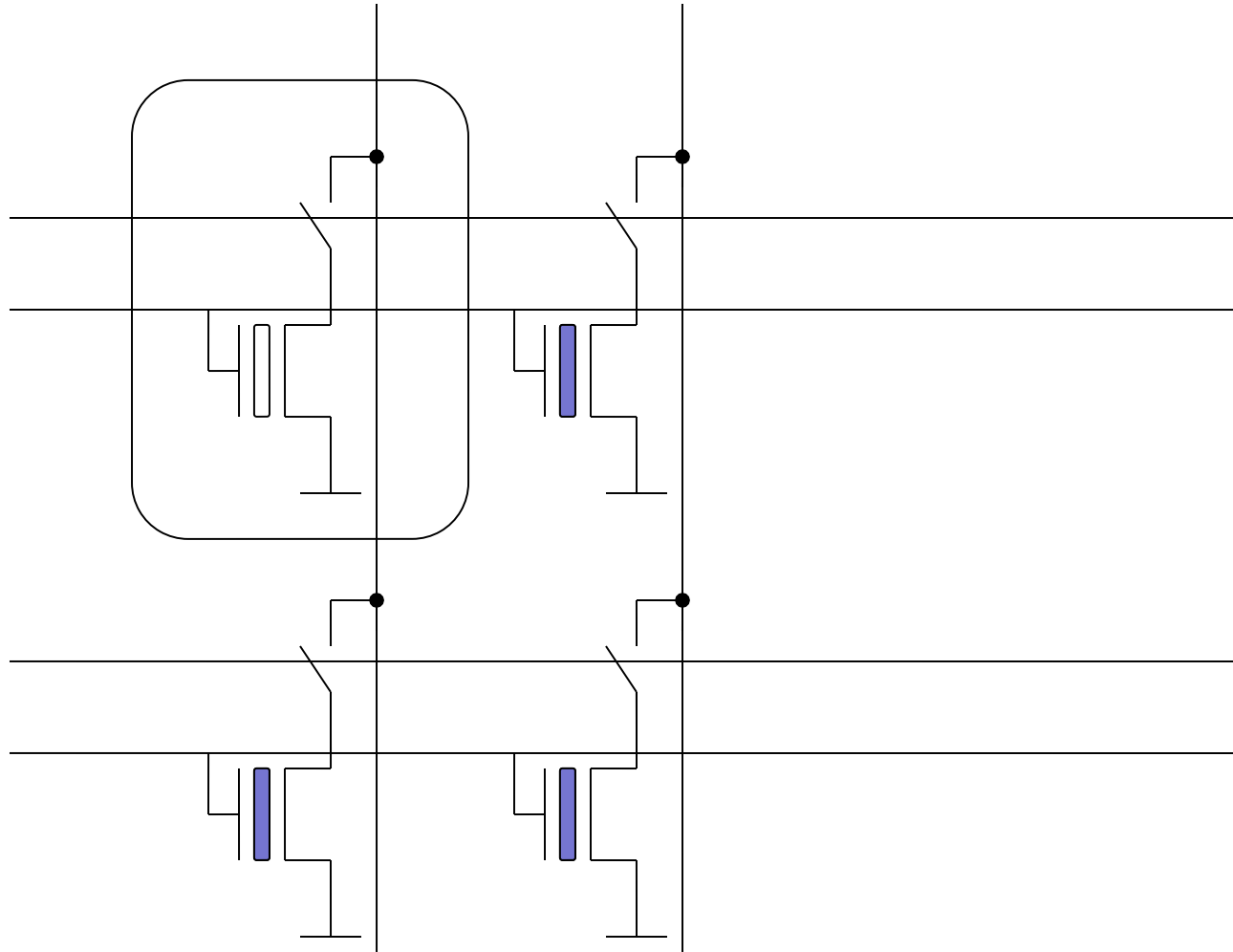
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



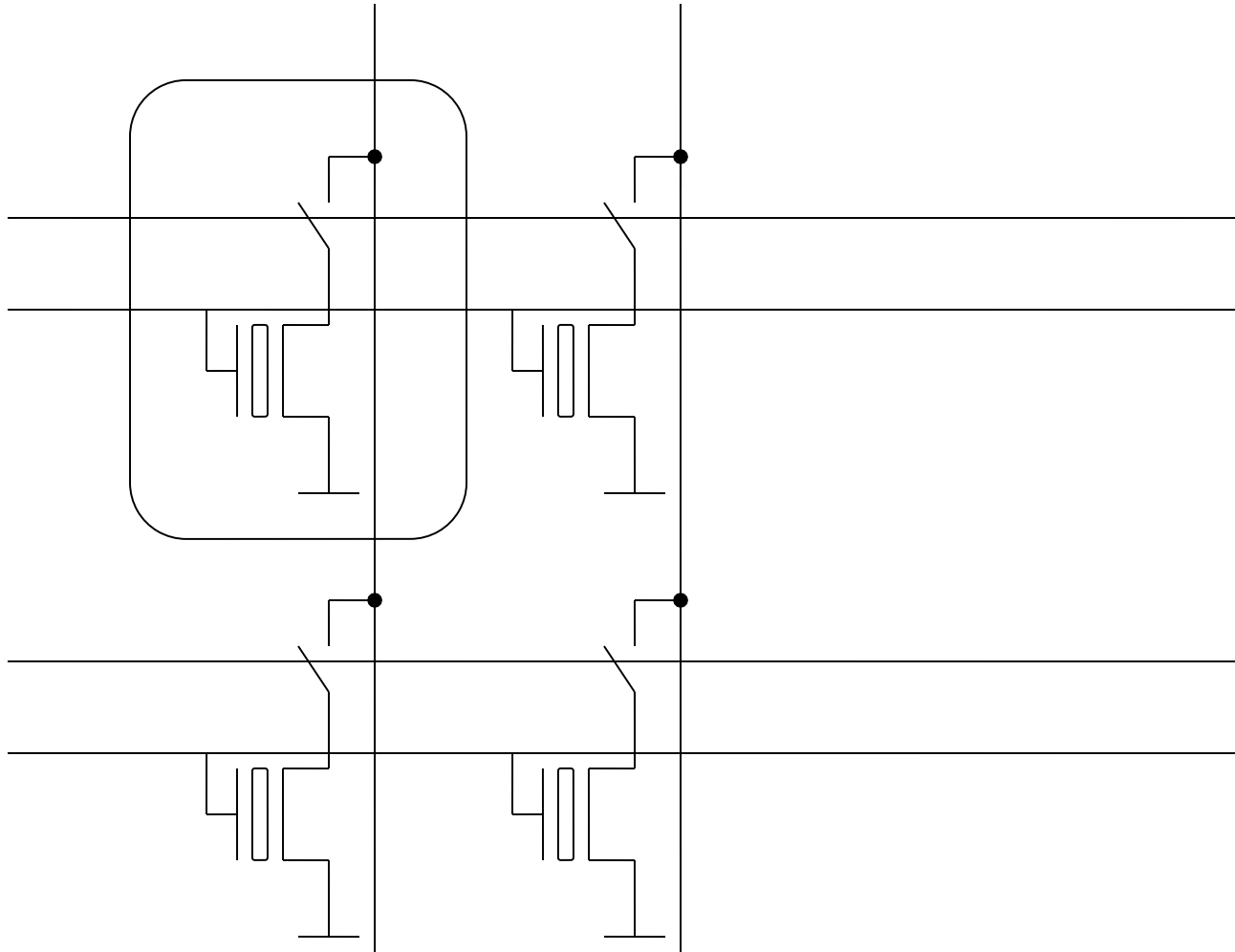
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



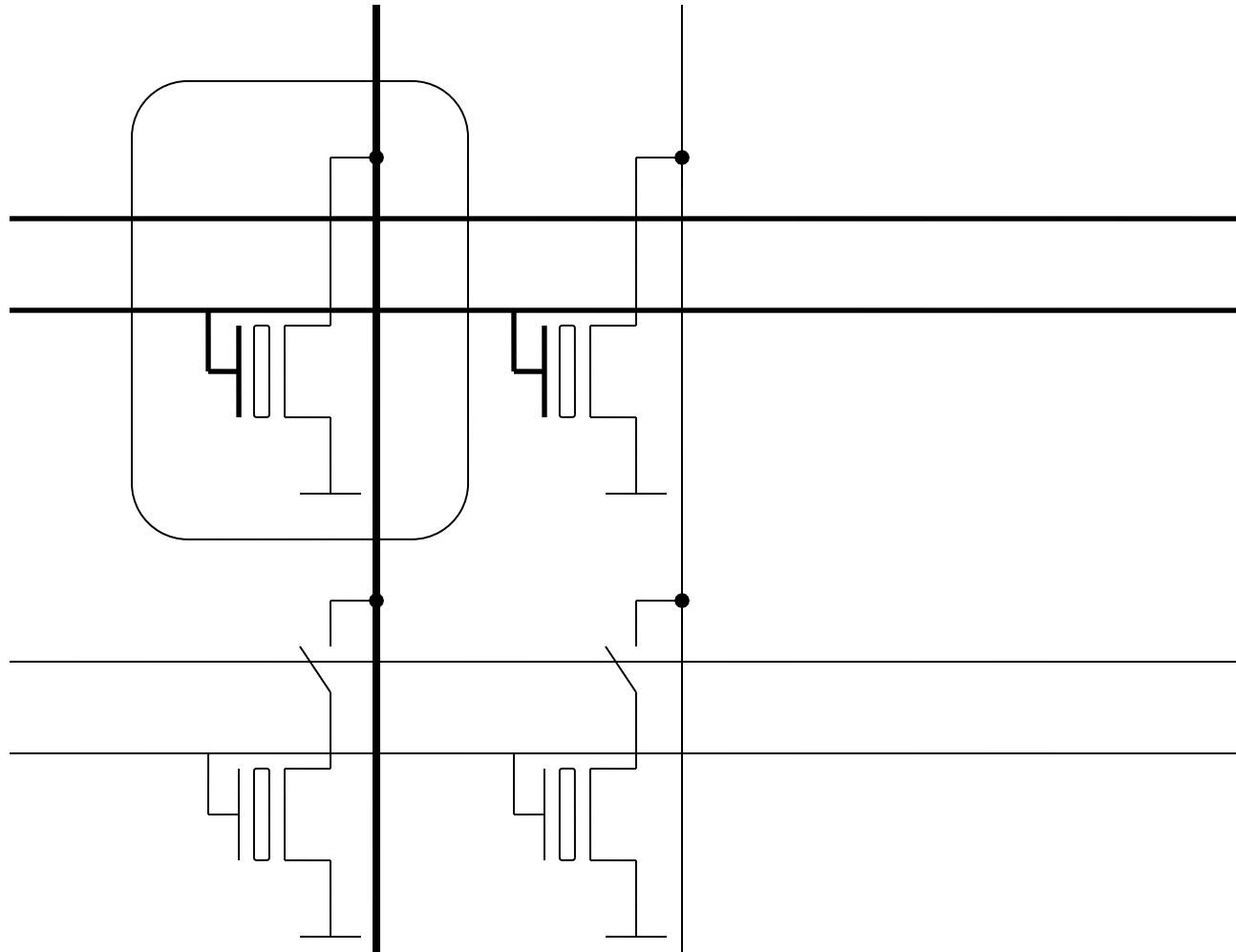
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



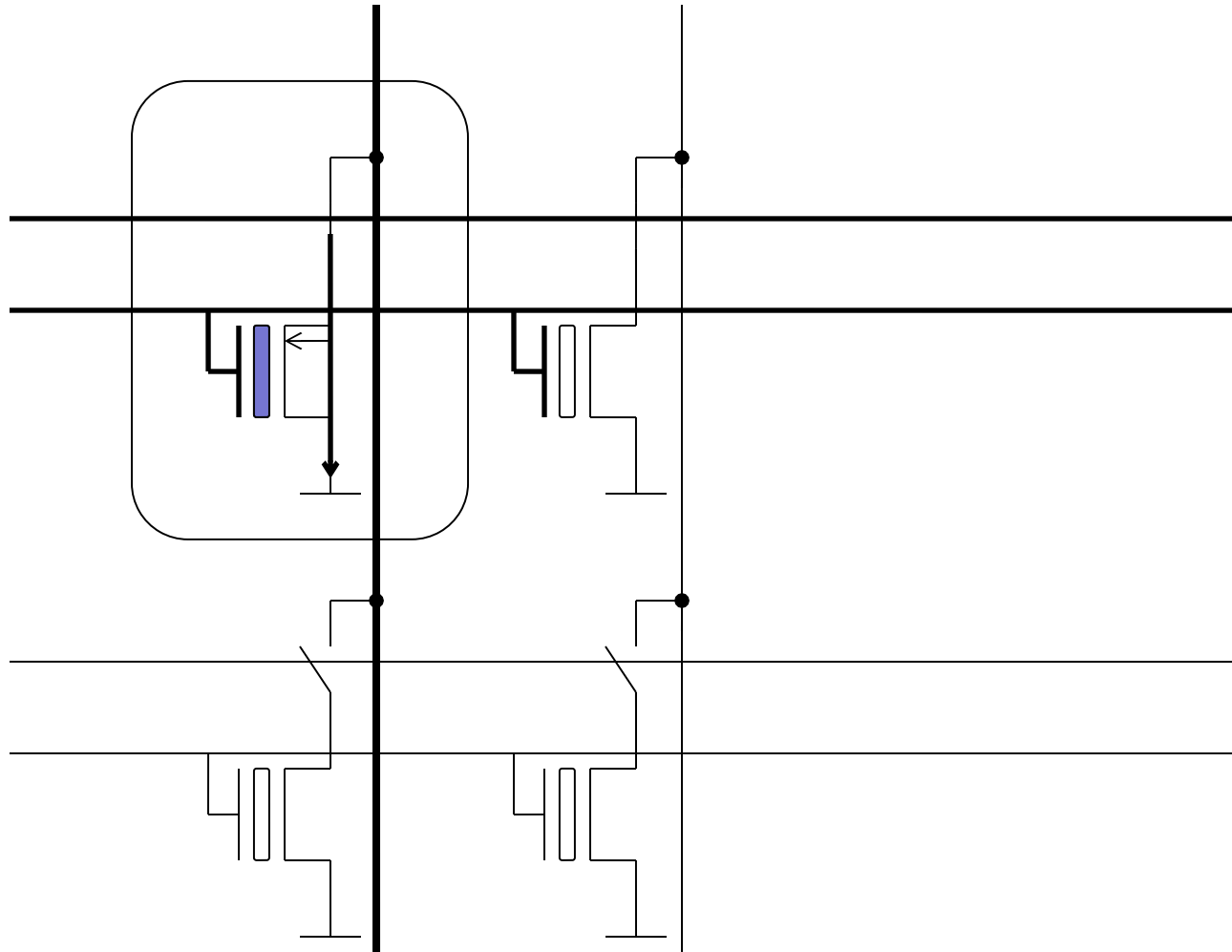
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



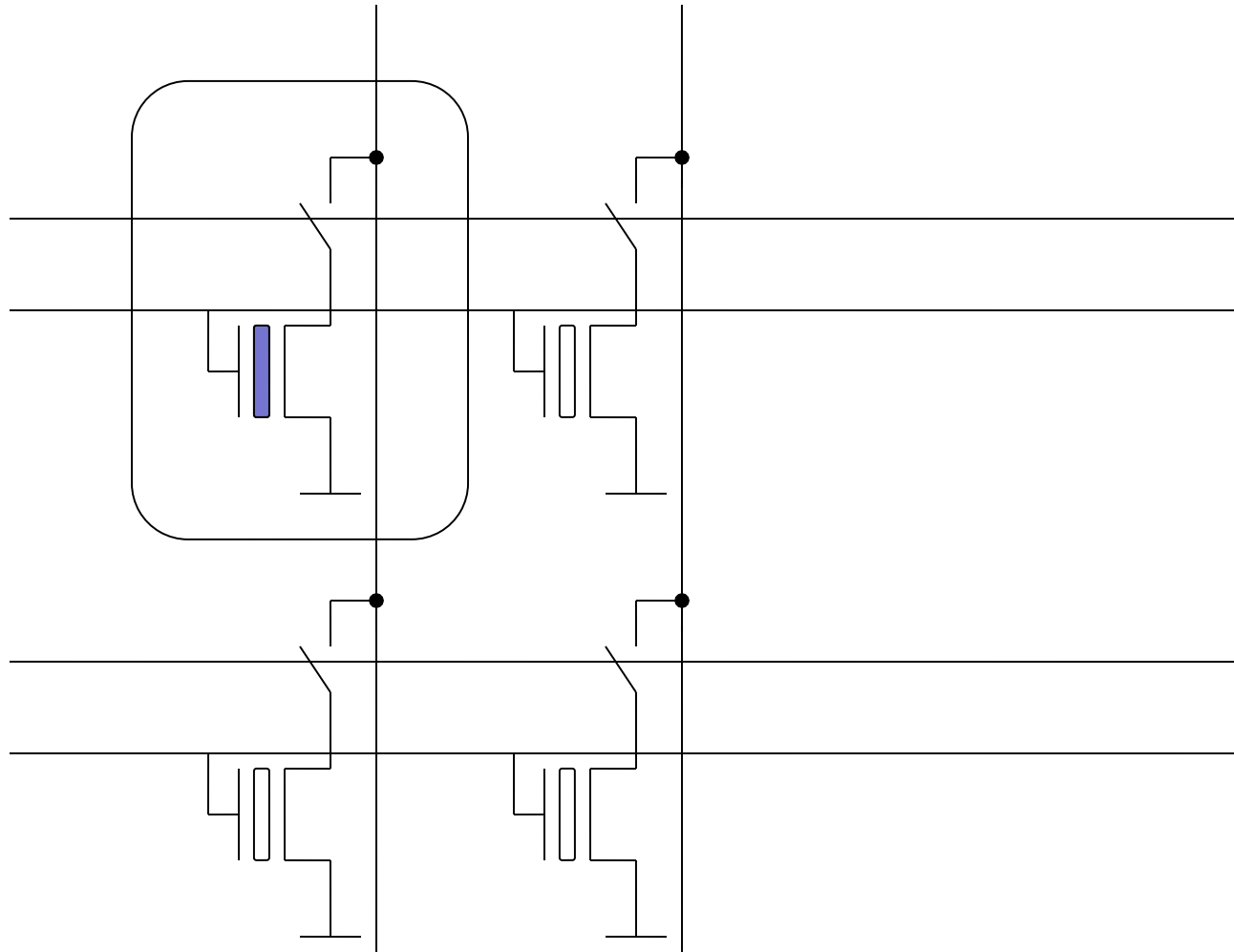
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



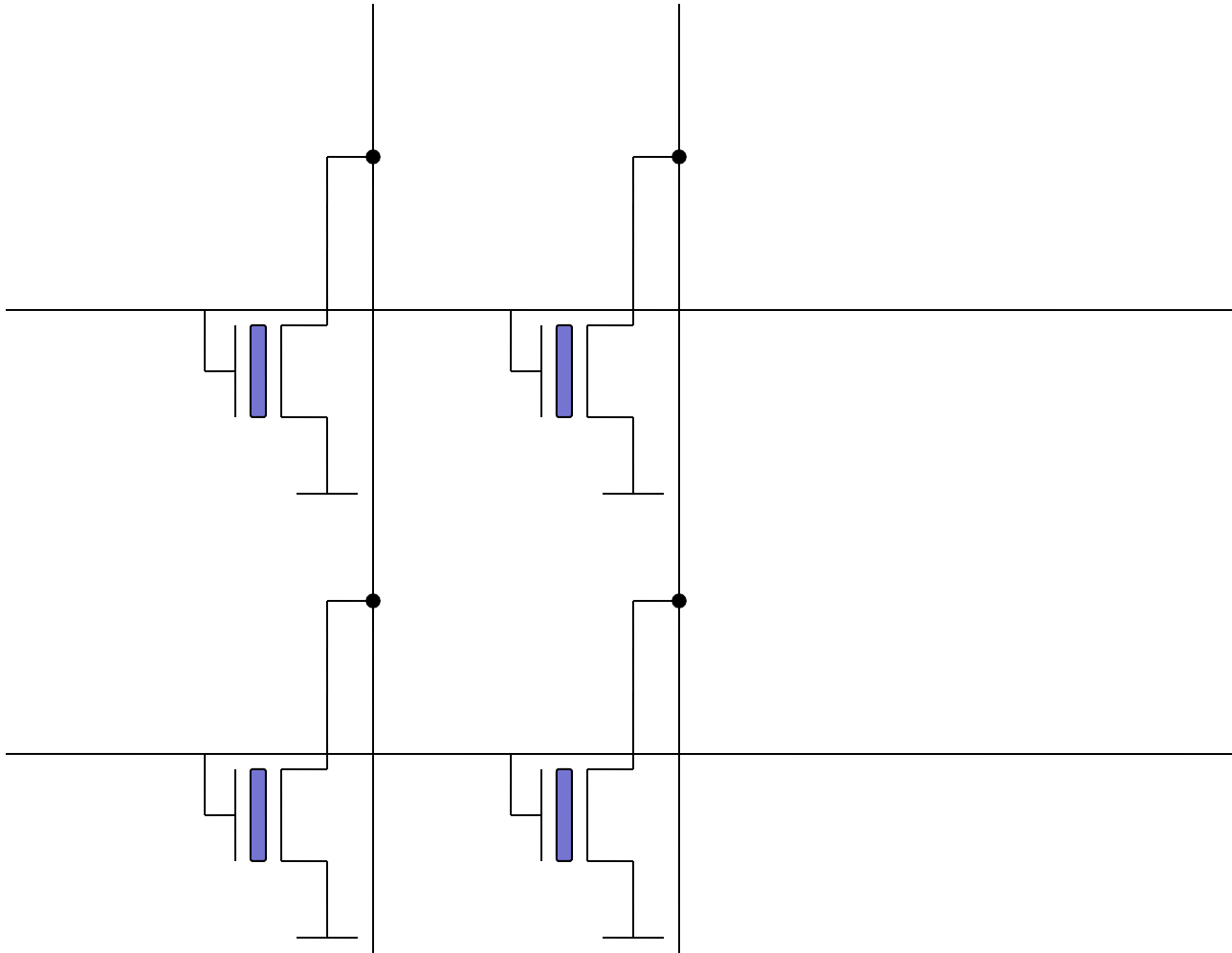
- EEPROM (erase based on tunnel effect, program based on hot carriers injection)



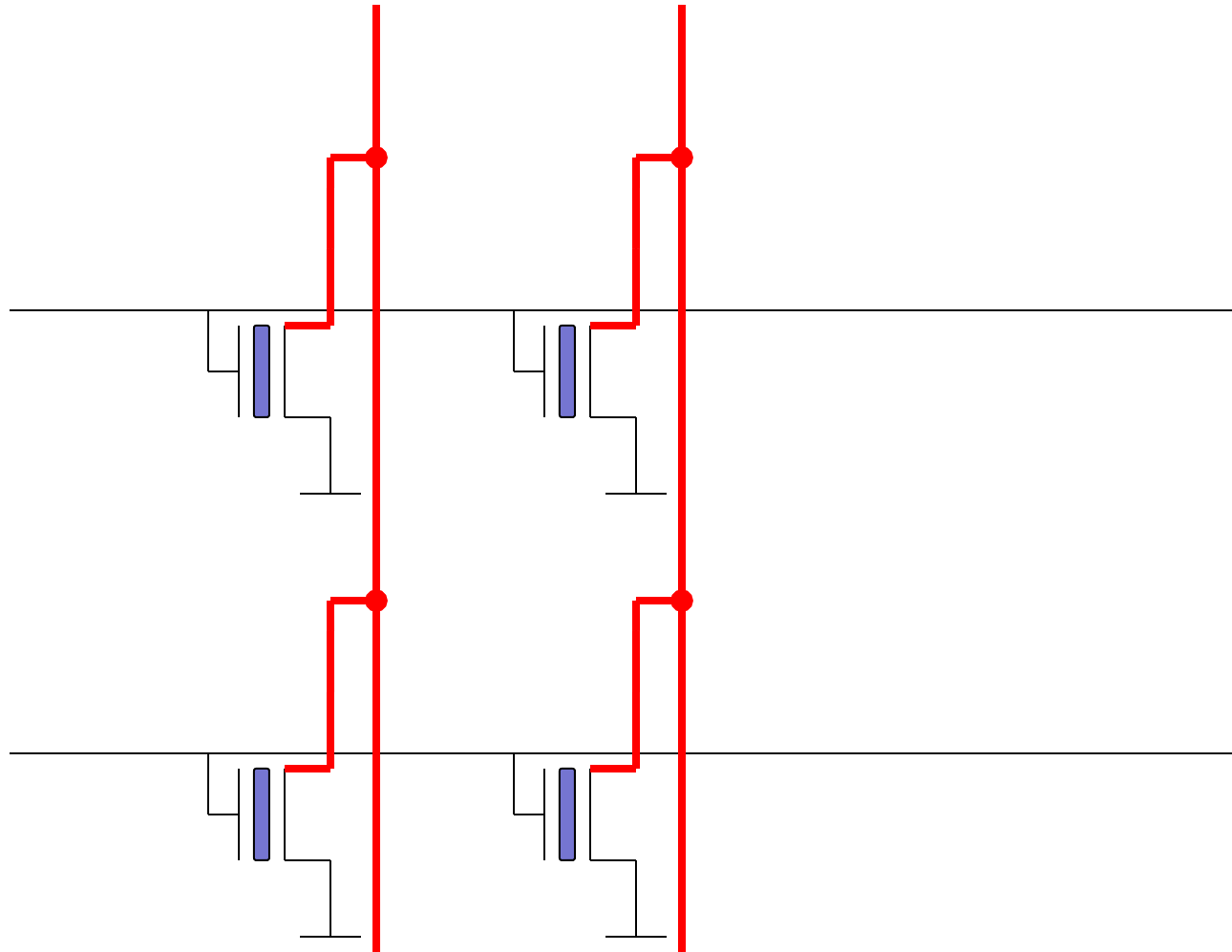
Variante 3

1 Transistor EEPROM (erase based on tunnel effect,
program based on hot carriers injection)

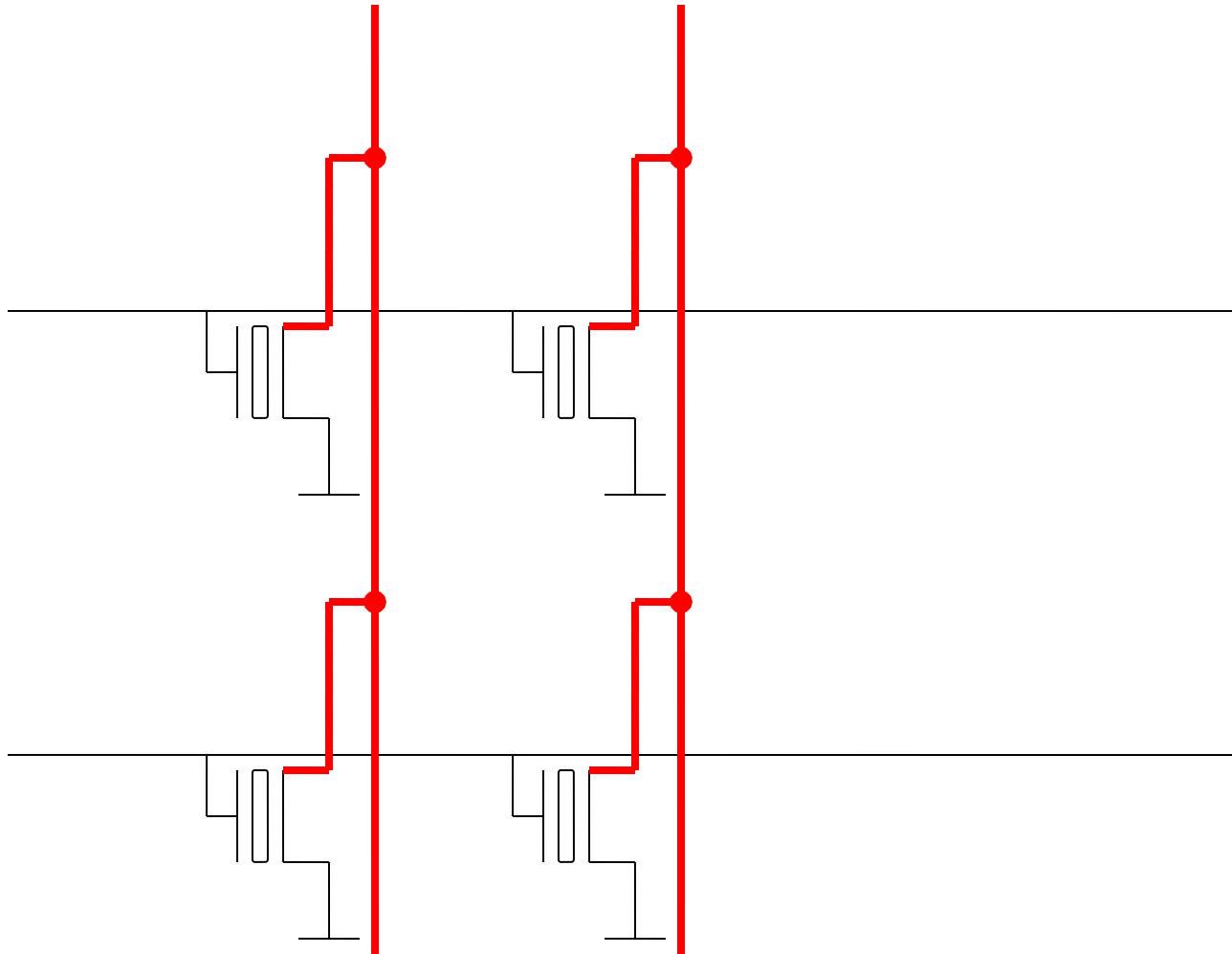
- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



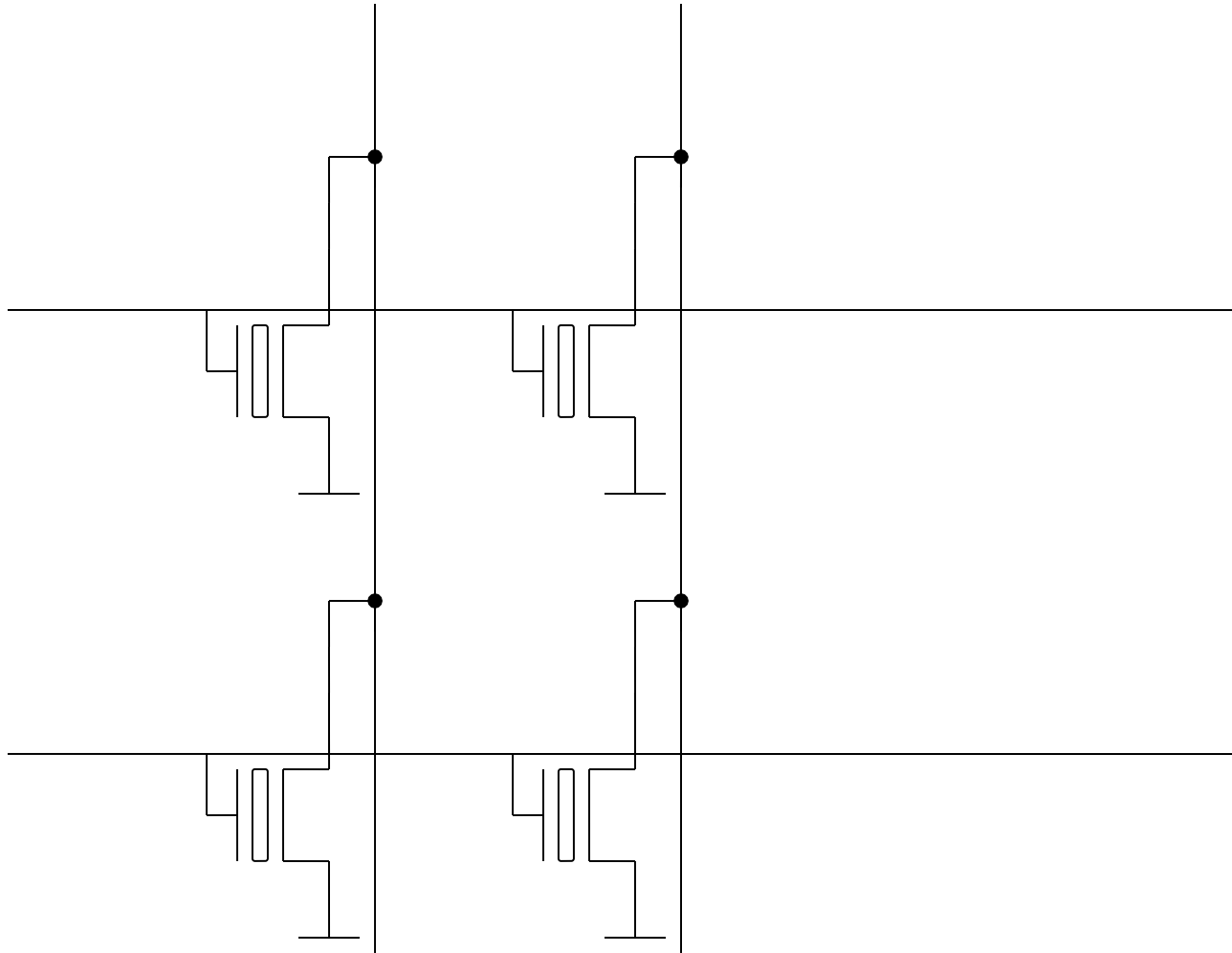
- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



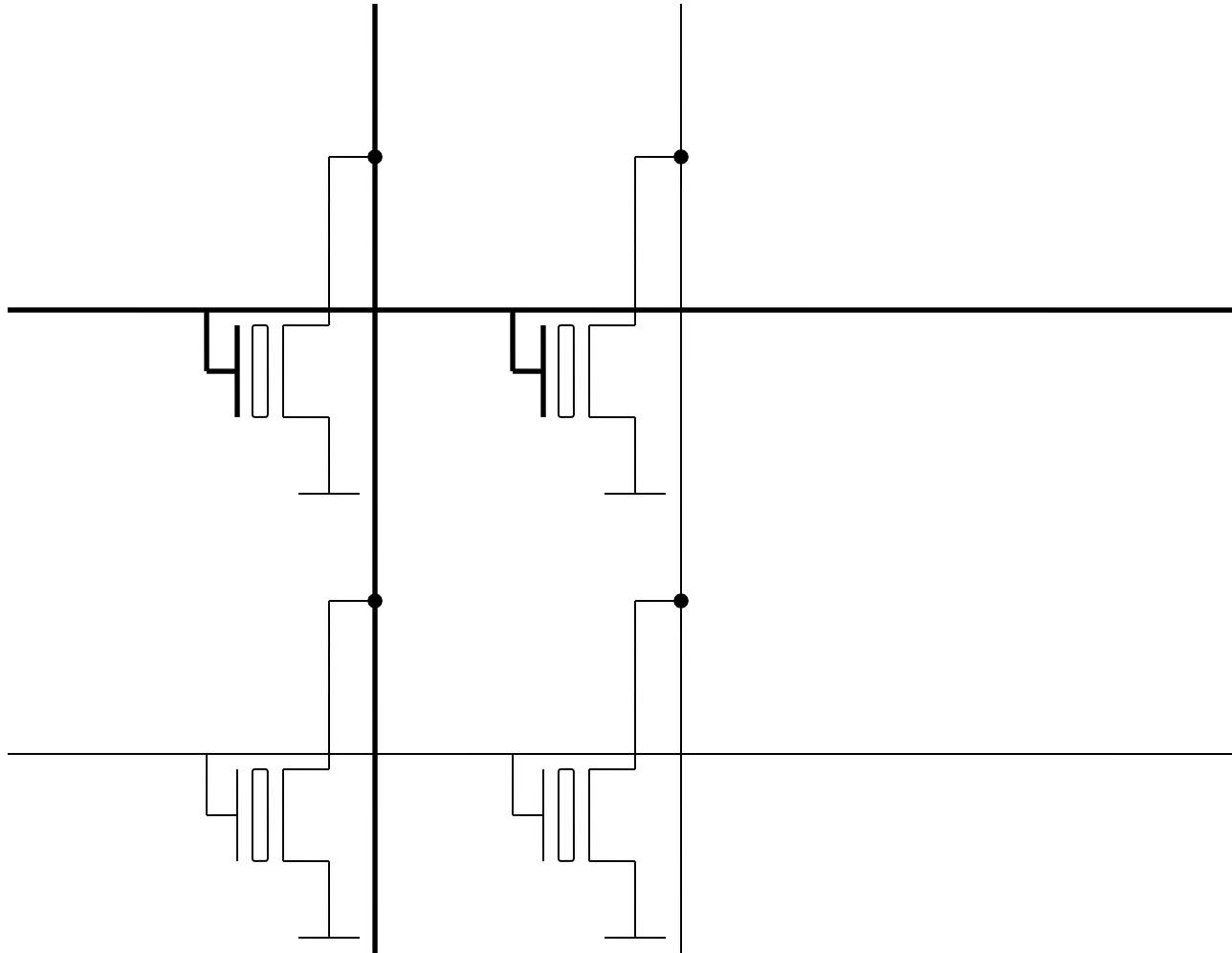
- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



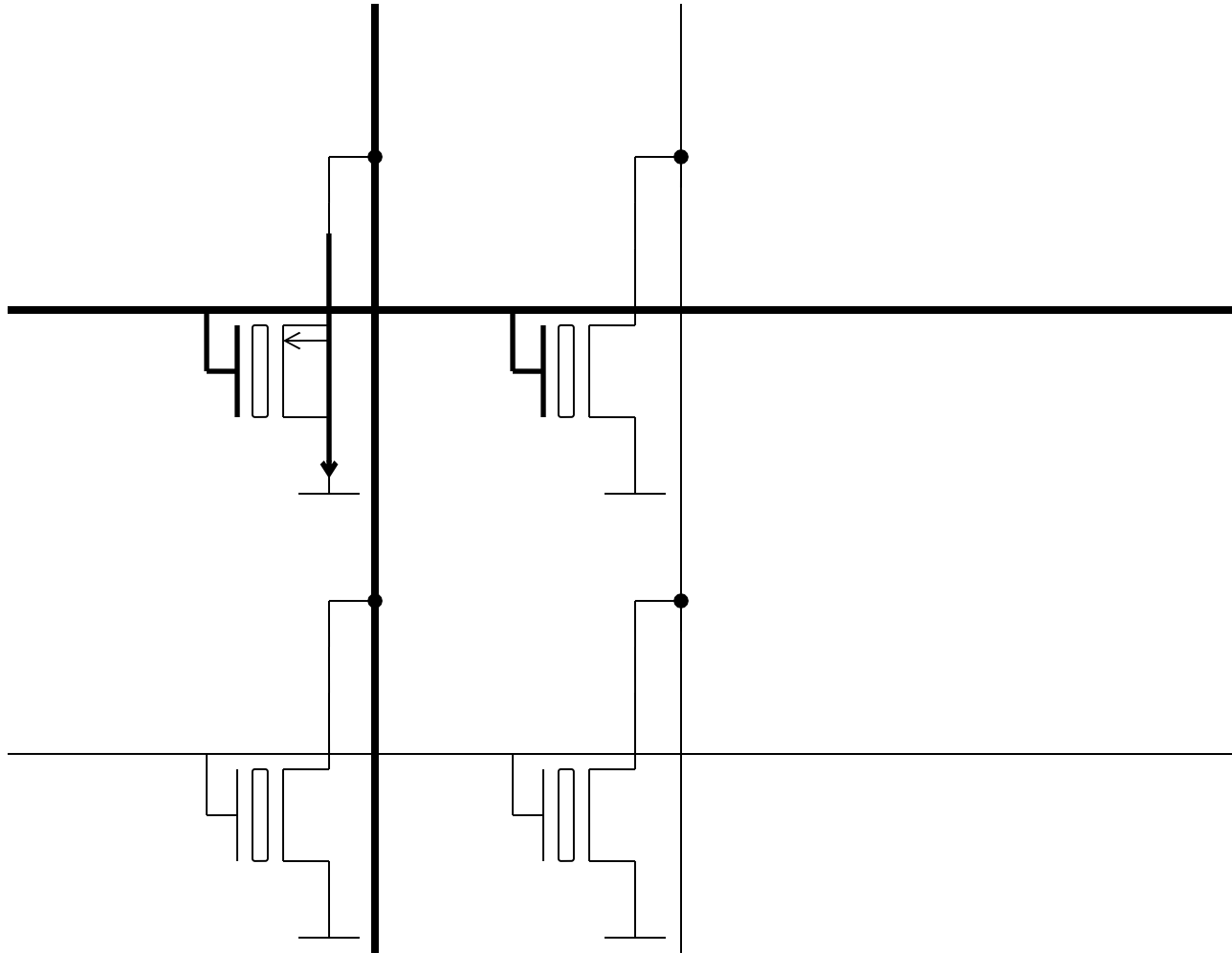
- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



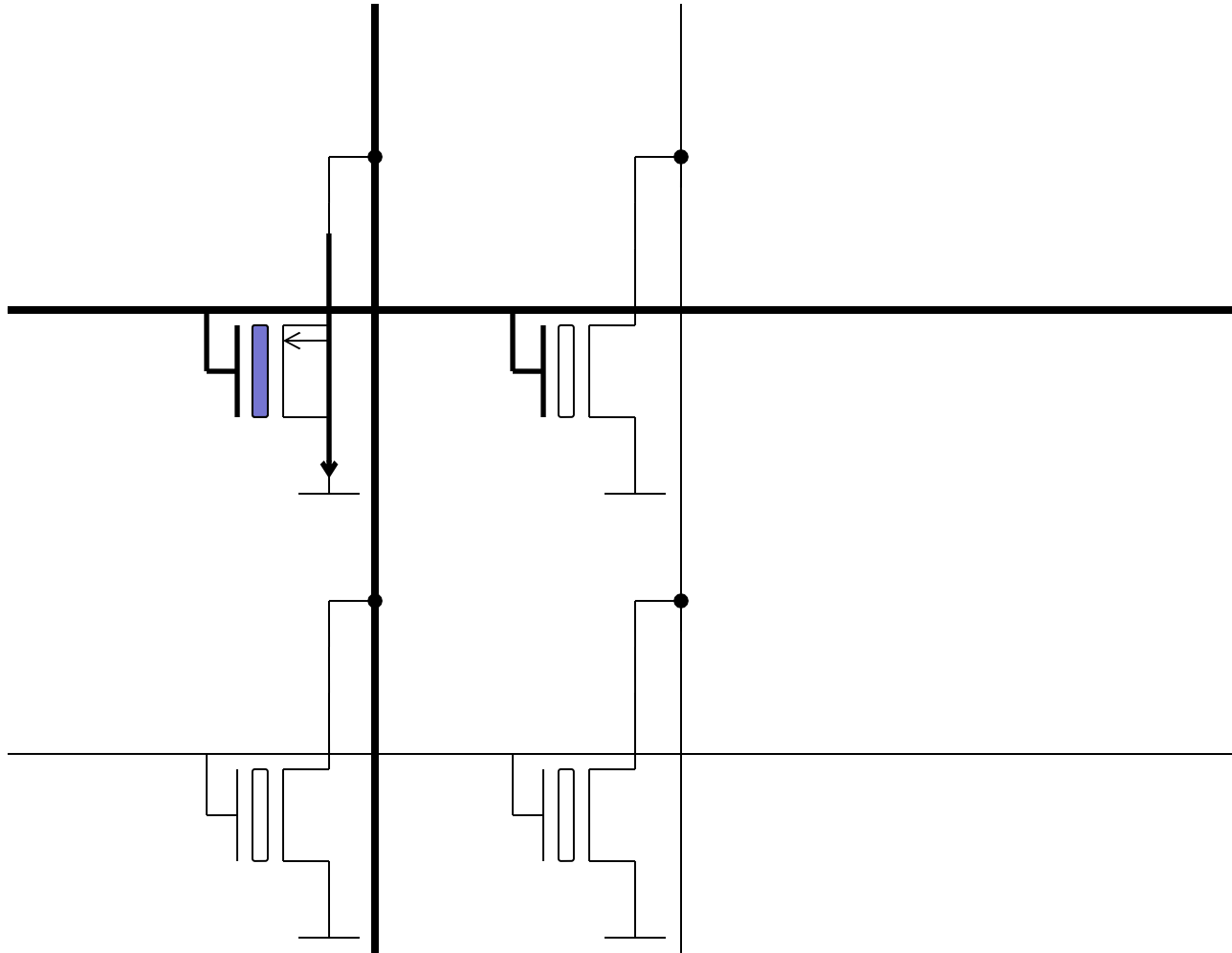
- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



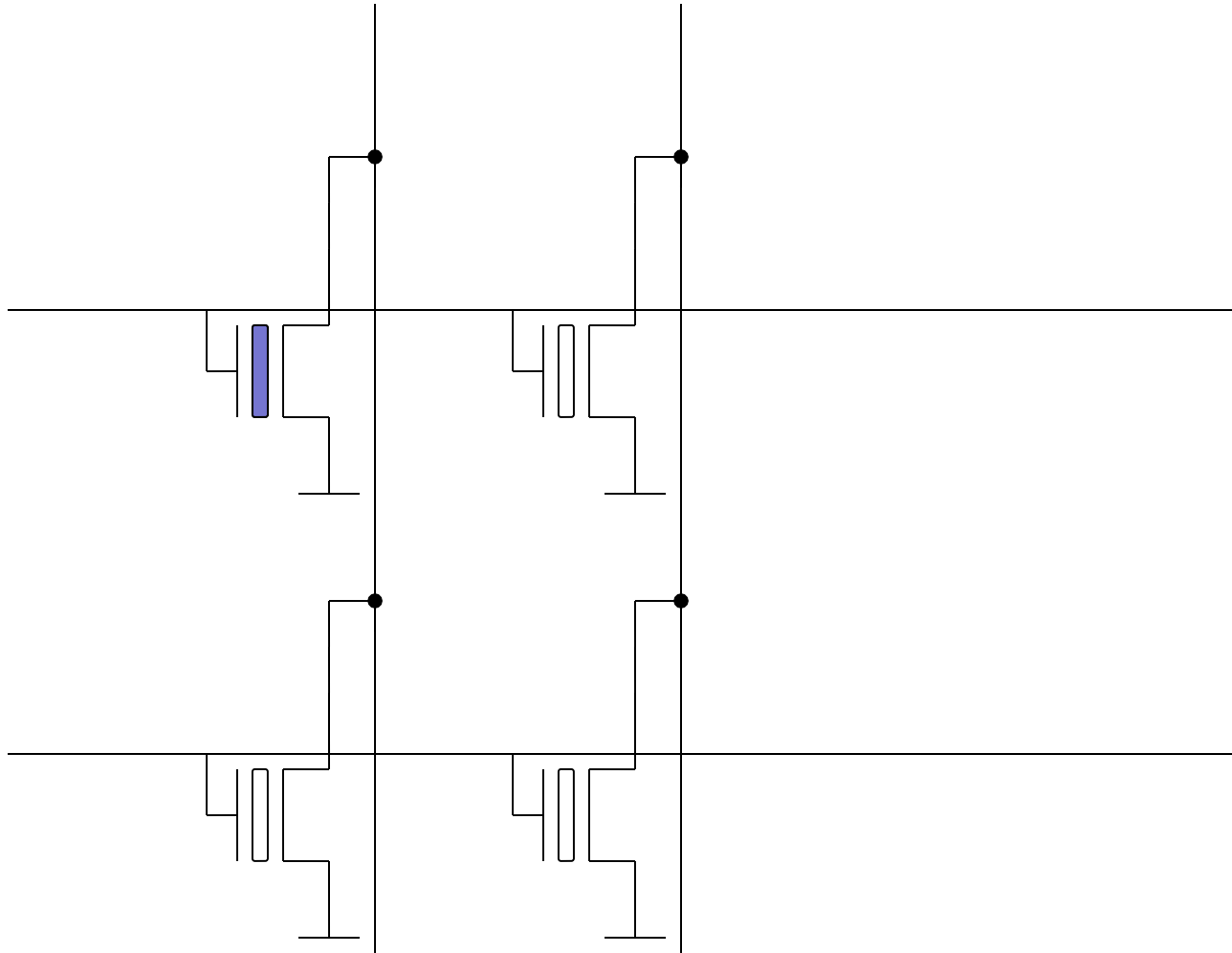
- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



- 1 Transistor EEPROM (erase based on tunnel effect, program based on hot carriers injection)



FLASH Speicher

Flash is a very popular term when it comes to storage media as it is used by portable devices like phones, tablets, and media players. **Flash actually is an offspring of EEPROM**, which stands for Electrically Erasable Programmable Read-Only Memory. **The main difference between EEPROM and Flash is the type of logic gates that they use. While EEPROM uses the faster NOR (a combination of Not and OR), Flash uses the slower NAND (Not and AND) type.** The NOR type is a lot faster than the NAND type but there is the matter of affordability as the former is significantly more expensive than the NAND type.

Another advantage of EEPROM over Flash is in how you can access and erase the stored data. EEPROM can access and erase the data byte-wise or a byte at a time. In comparison, Flash can only do so block-wise. In order to simplify the whole thing, individual bytes are grouped into a smaller number of blocks, which can have thousands of bytes in each block. This is a bit problematic when you only want to read or write to a single byte at a time; which is what's typically needed in executing the code of a program. This is a reason why Flash cannot be used in electronic circuits that require byte-wise access to data. Data in Flash can also be executed, but it needs to be read as a whole and loaded into RAM beforehand.

EEPROM was designed to be read a lot more than it is written. This is in-line with programming for electronic circuits where you write to the chip a number of times while testing the program. Then, it is stored for good, only to be read every time the data is needed. This is not very suitable for storage media where data is routinely written and read.

In typical use, Flash is used mainly to refer to storage media and can range anywhere from a GB to hundreds of GB. In contrast, EEPROM is usually reserved for permanent code storage in electronic chips. Typical values range from kilobytes to a couple of megabytes.

Summary:

- 1. Flash is just one type of EEPROM**
- 2. Flash uses NAND type memory while EEPROM uses NOR type**
- 3. Flash is block-wise erasable while EEPROM is byte-wise erasable**
- 4. Flash is constantly rewritten while other EEPROMs are seldom rewritten**
- 5. Flash is when large amounts are needed while EEPROM is used when only small amounts are needed**

Der Mechanismus, der die Elektronen durch die isolierende Oxidschicht passieren lässt, wird **Fowler-Nordheim-Tunneleffekt** genannt (nach ihren ersten Erforschern), d. h. bei einem Flashspeicher handelt es sich um die Anwendung eines nur quantenmechanisch deutbaren Effekts. Um die Wahrscheinlichkeit, dass Elektronen zum Floating-Gate tunneln, zu erhöhen, wird oft das Verfahren **CHE (engl. *channel hot electron*)** verwendet: Die Elektronen werden durch Anlegen einer Spannung über dem Kanal, also zwischen Drain und Source, beschleunigt und dadurch auf ein höheres Energieniveau (daher engl. *hot*) gehoben, wodurch sie schon bei geringeren Spannungen (typischerweise 10 V) zwischen Gate und Kanal zum Floating-Gate tunneln.

Ein Flash-Speicher besteht aus einer bestimmten, von der Speichergröße abhängigen Anzahl einzelner Speicherelemente. Die Bytes oder Worte (typisch durchaus bis 64 Bit) können einzeln adressiert werden.

Dabei können sie in einigen Architekturen auch einzeln geschrieben werden, wogegen bei anderen nur größere Datenmengen auf einmal programmiert werden können. In der Regel ist die entgegengesetzte Operation, das Löschen, aber nur in größeren Einheiten, sogenannten Sektoren (meistens ein Viertel, Achtel, Sechzehntel usw. der Gesamtspeicherkapazität) möglich.

Flash-Speicher haben eine begrenzte Lebensdauer, die in einer maximalen Anzahl an Löschzyklen angegeben wird (10.000 bis 100.000 Zyklen für NOR-Flash und bis zu zwei Millionen für NAND-Flash).

Dies entspricht gleichzeitig der maximalen Anzahl Schreibzyklen, da der Speicher jeweils blockweise gelöscht werden muss, bevor er wieder beschrieben werden kann. Diese Zyklenzahl wird Endurance (Beständigkeit) genannt. Verantwortlich für diese begrenzte Lebensdauer ist das Auftreten von Schäden in der Oxidschicht im Bereich des Floating-Gates, was das Abfließen der Ladung bewirkt.^[3]

Eine andere wichtige Kenngröße ist die Zeit der fehlerfreien Datenhaltung, die Retention.

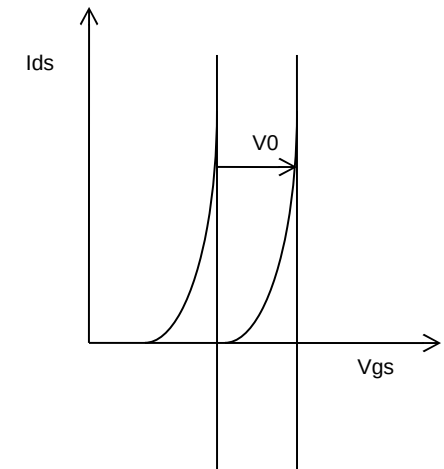
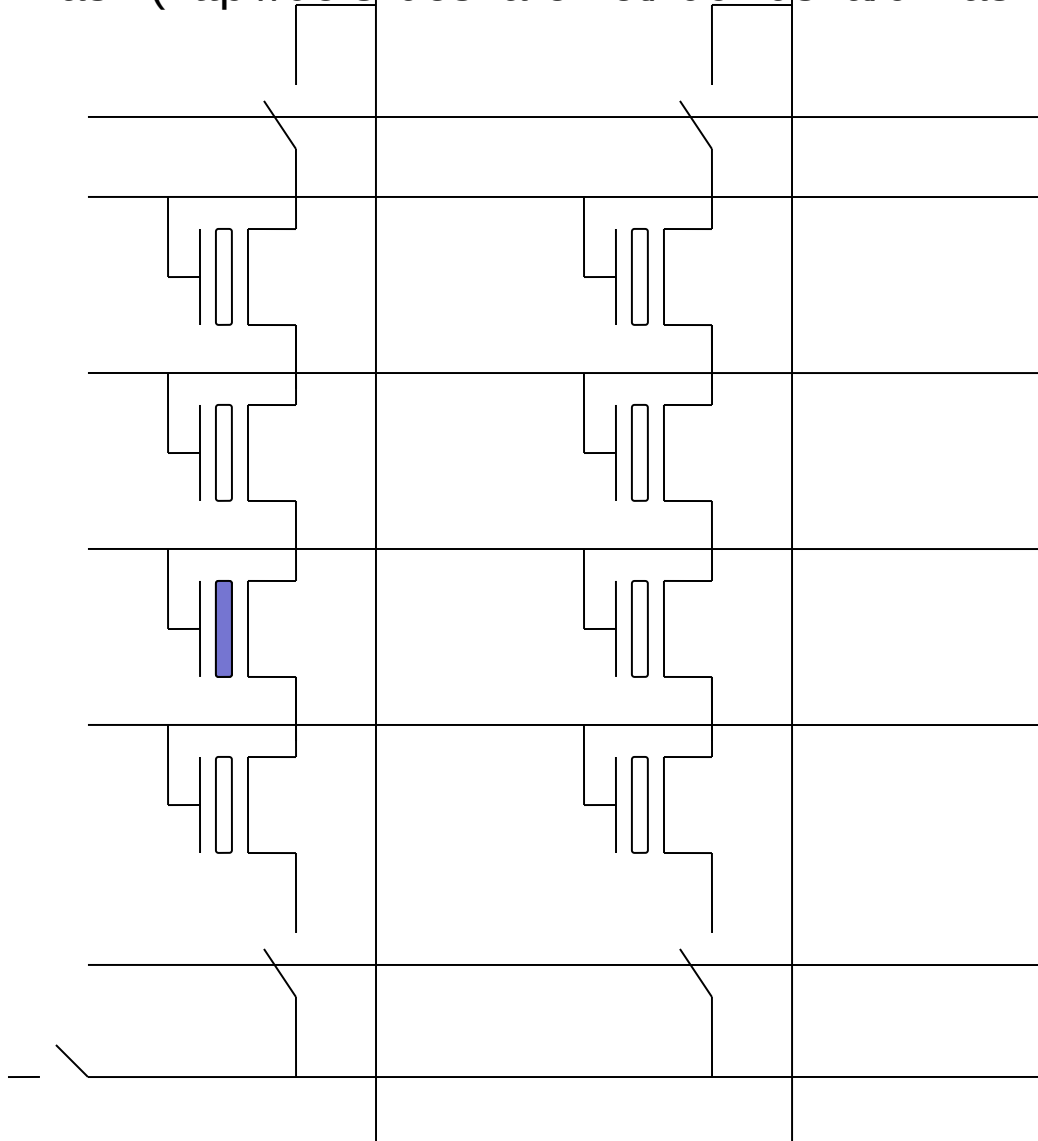
Ein weiterer Nachteil ist, dass der Schreibzugriff bei Flash-Speicher erheblich langsamer erfolgt als der Lesezugriff. Zusätzliche Verzögerungen können dadurch entstehen, dass immer nur ganze Blöcke gelöscht werden können.

Der Flash-Speicher speichert seine Informationen auf dem Floating-Gate. Bei einem Löschzyklus durchtunneln die Elektronen die Oxidschicht. **Dafür sind hohe Spannungen erforderlich. Dadurch wird bei jedem Löschvorgang die Oxidschicht, die das Floating-Gate umgibt, ein klein wenig beschädigt (Degeneration).** Irgendwann ist die Isolation durch die Oxidschicht nicht mehr gegeben, die Elektronen bleiben nicht mehr auf dem Floating-Gate gefangen, und die auf der Speicherzelle gespeicherte Information geht verloren. Der Defekt einer einzelnen Zelle macht einen Flash-Speicher jedoch noch lange nicht unbrauchbar.

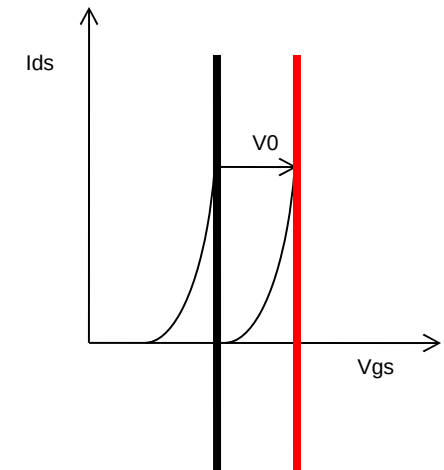
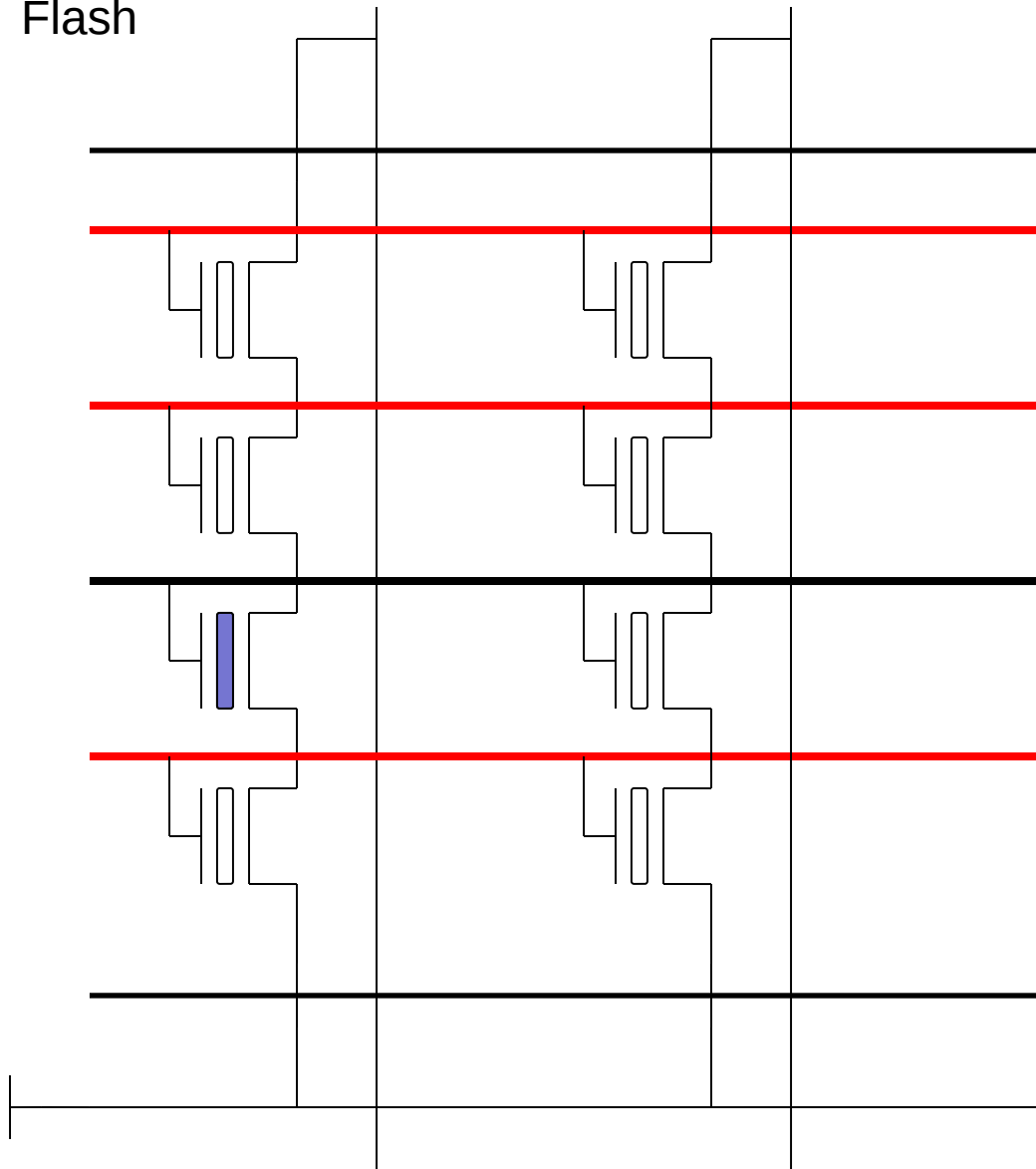
Als nichtflüchtiges Speichermedium steht der Flash-Speicher in Konkurrenz vor allem zu Festplatten und optischen Speichern wie [DVDs](#) und [Blu-ray-Discs](#).

Ein wesentlicher Vorteil liegt in der mechanischen Robustheit von Flash-Speicher. Demgegenüber sind Festplatten sehr stoßempfindlich ([Head-Crash](#)). Häufig ist die [Lebensdauer](#) der Steckkontakte ([USB-Stecker](#)) der [limitierende Faktor](#).

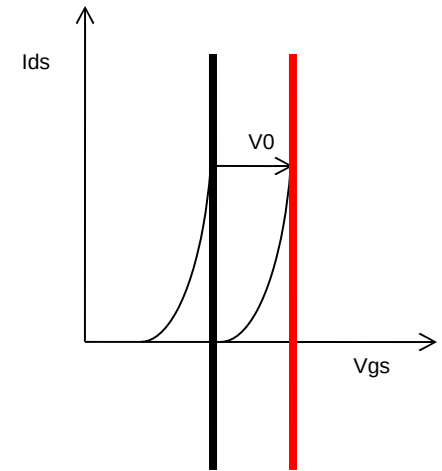
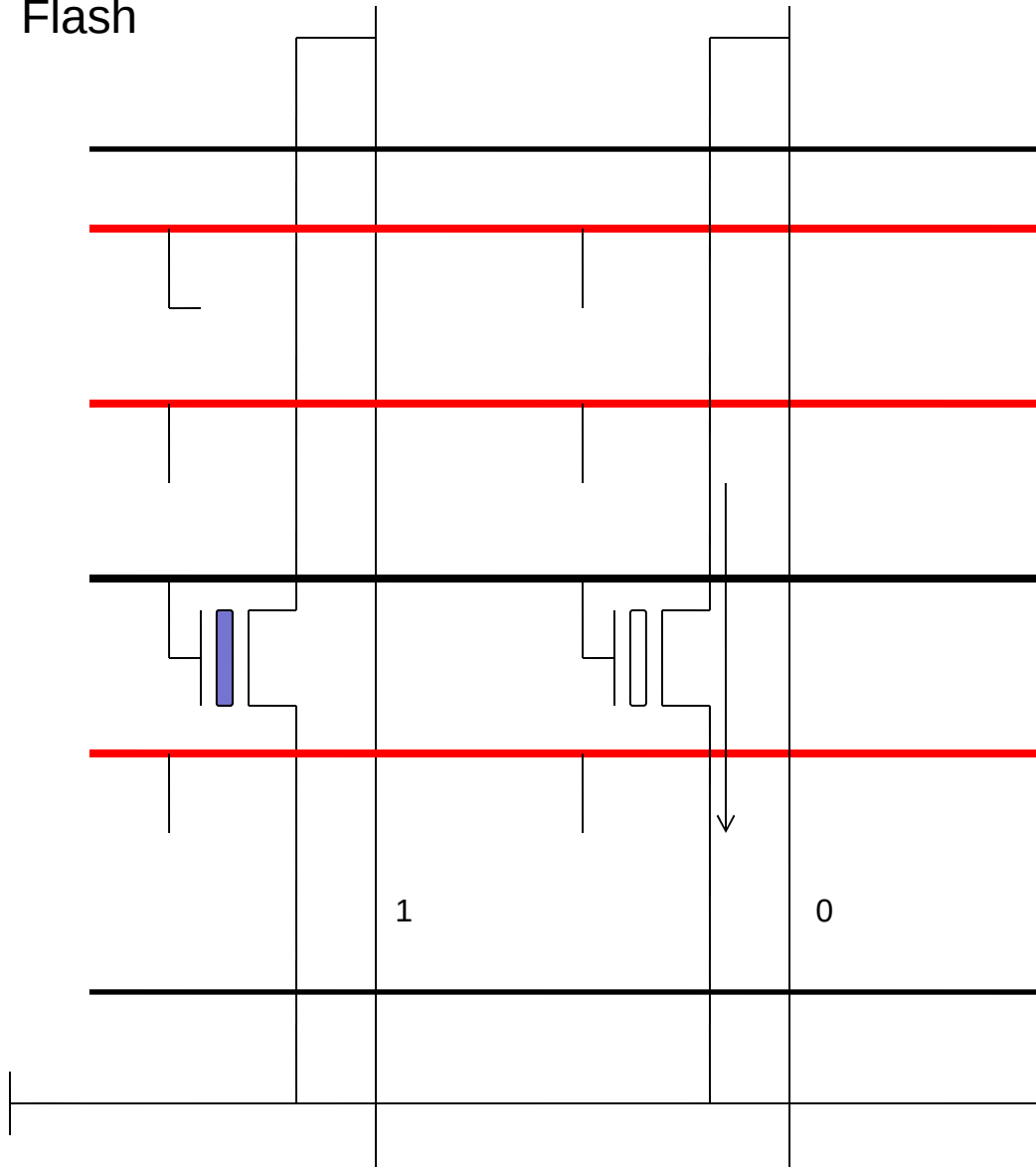
- Flash (<http://de.slideshare.net/ruchiusha/07flash-memory-technology>)



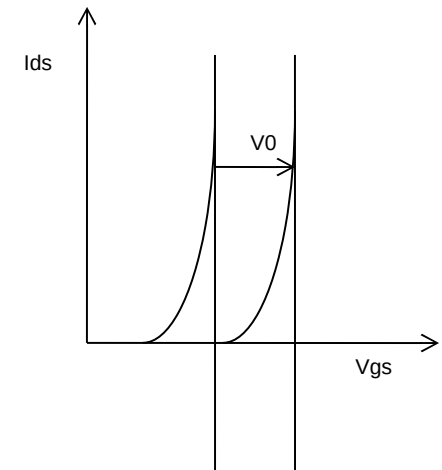
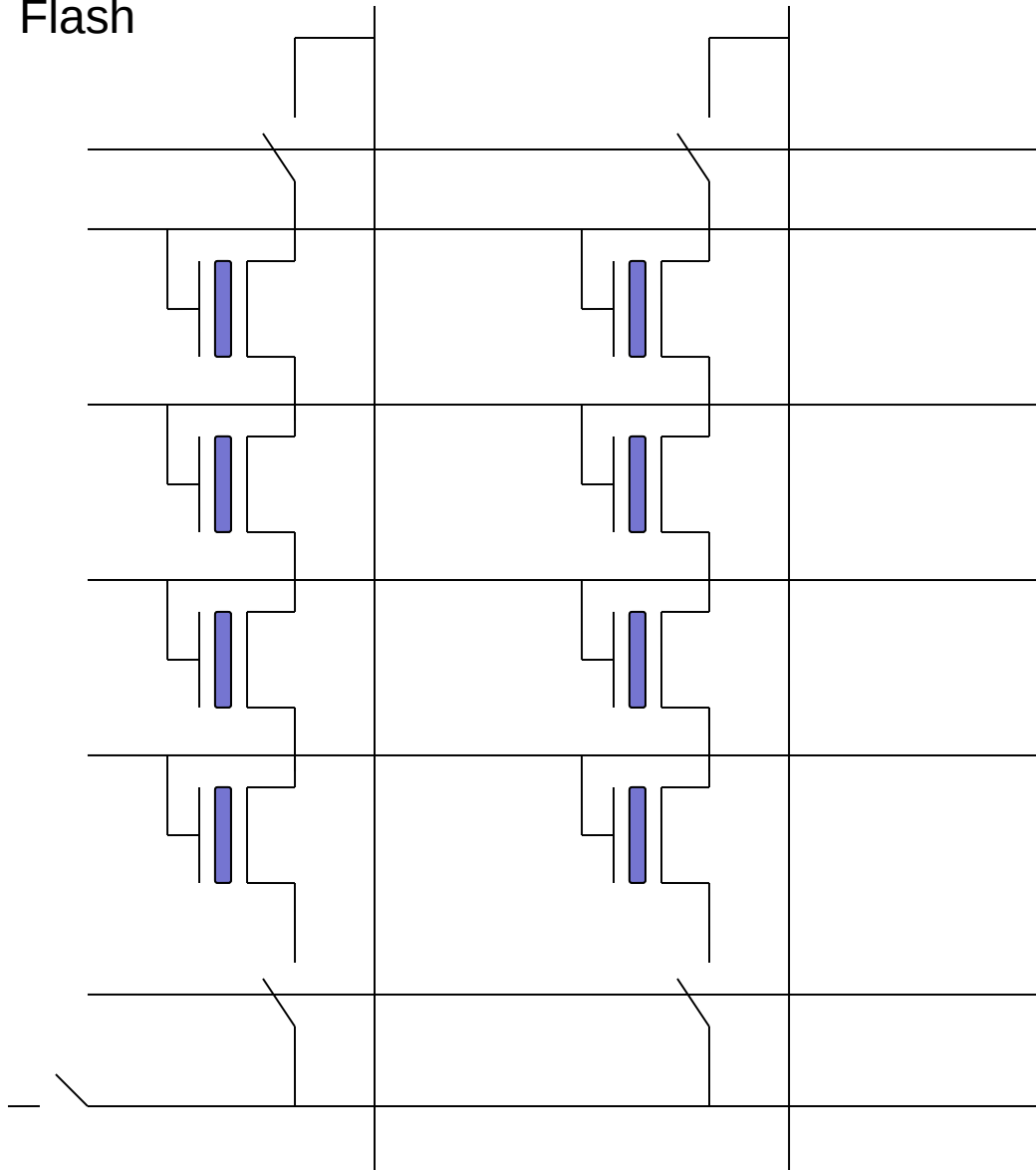
- Flash



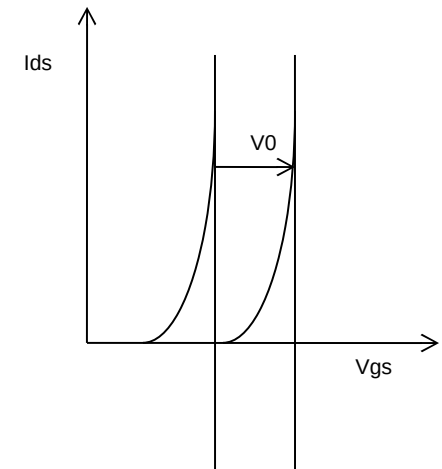
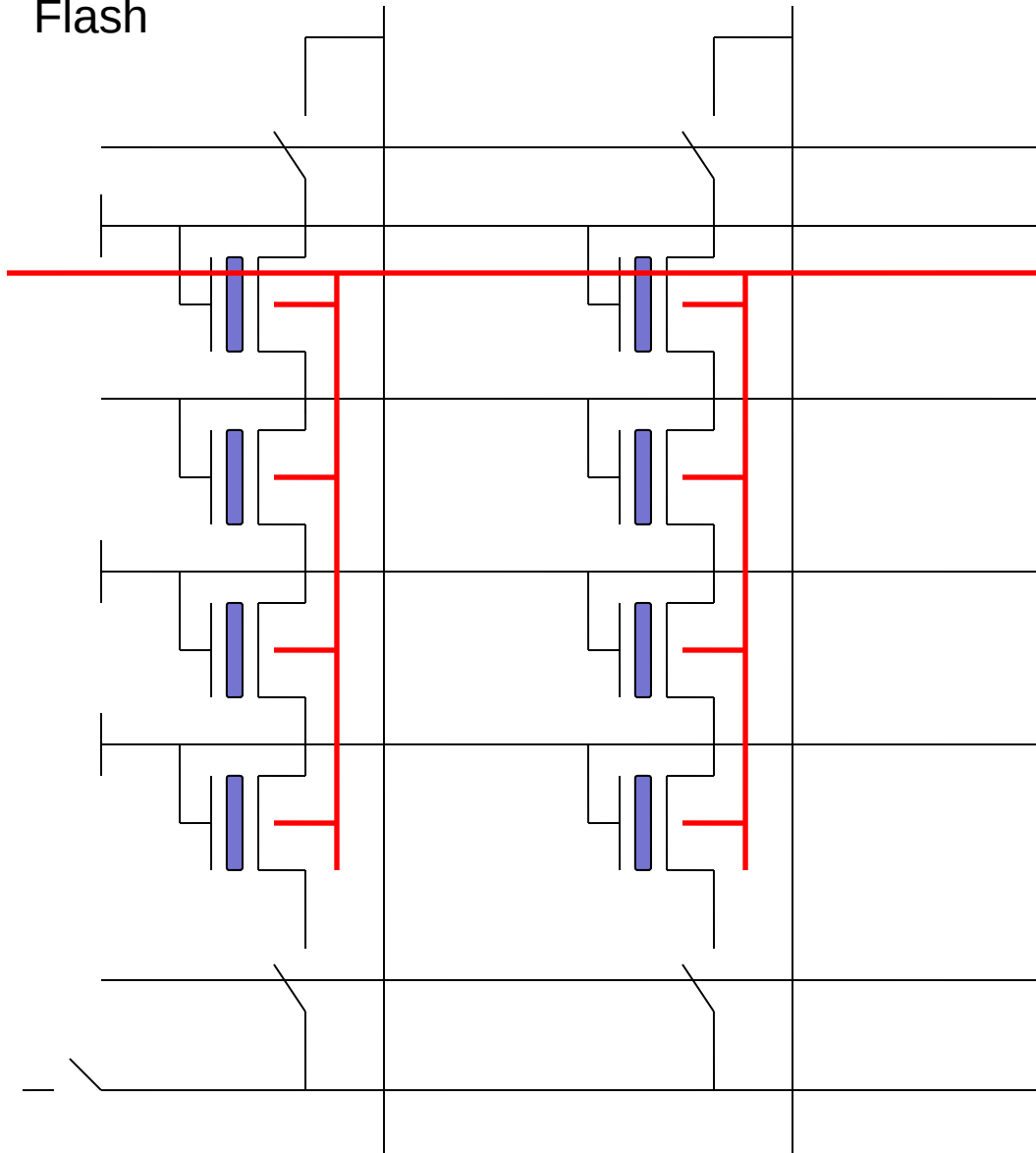
- Flash



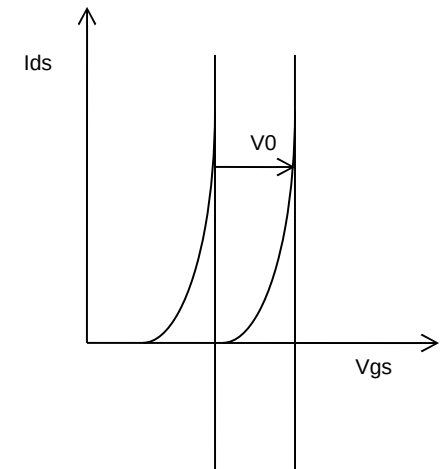
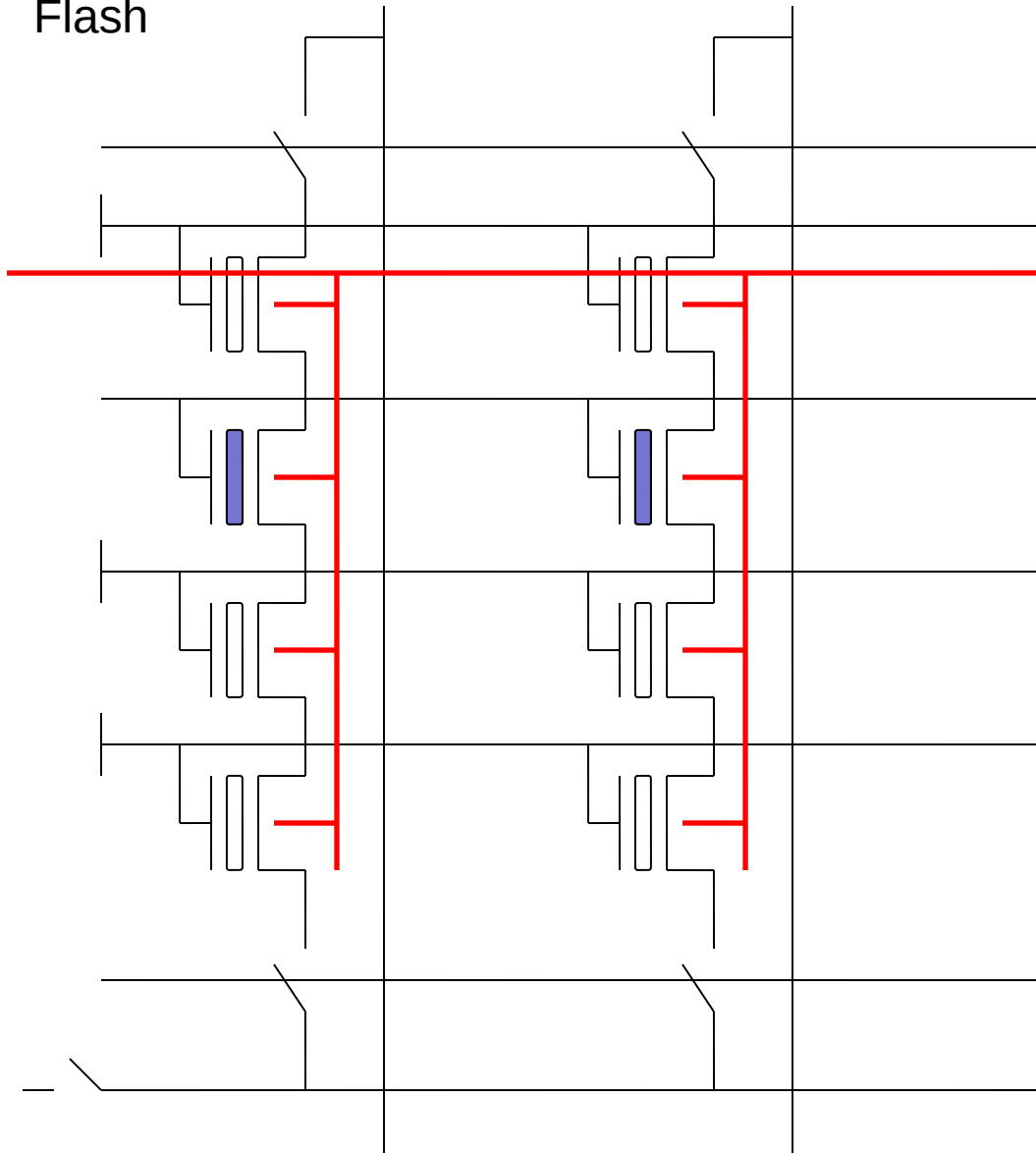
- Flash



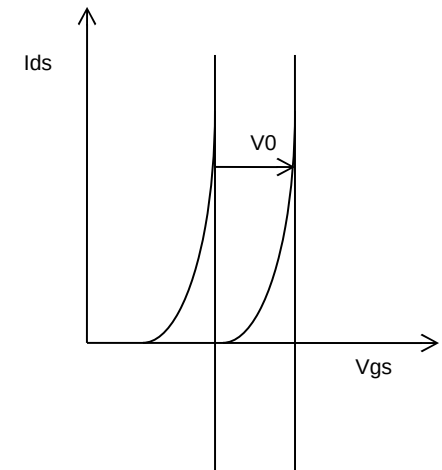
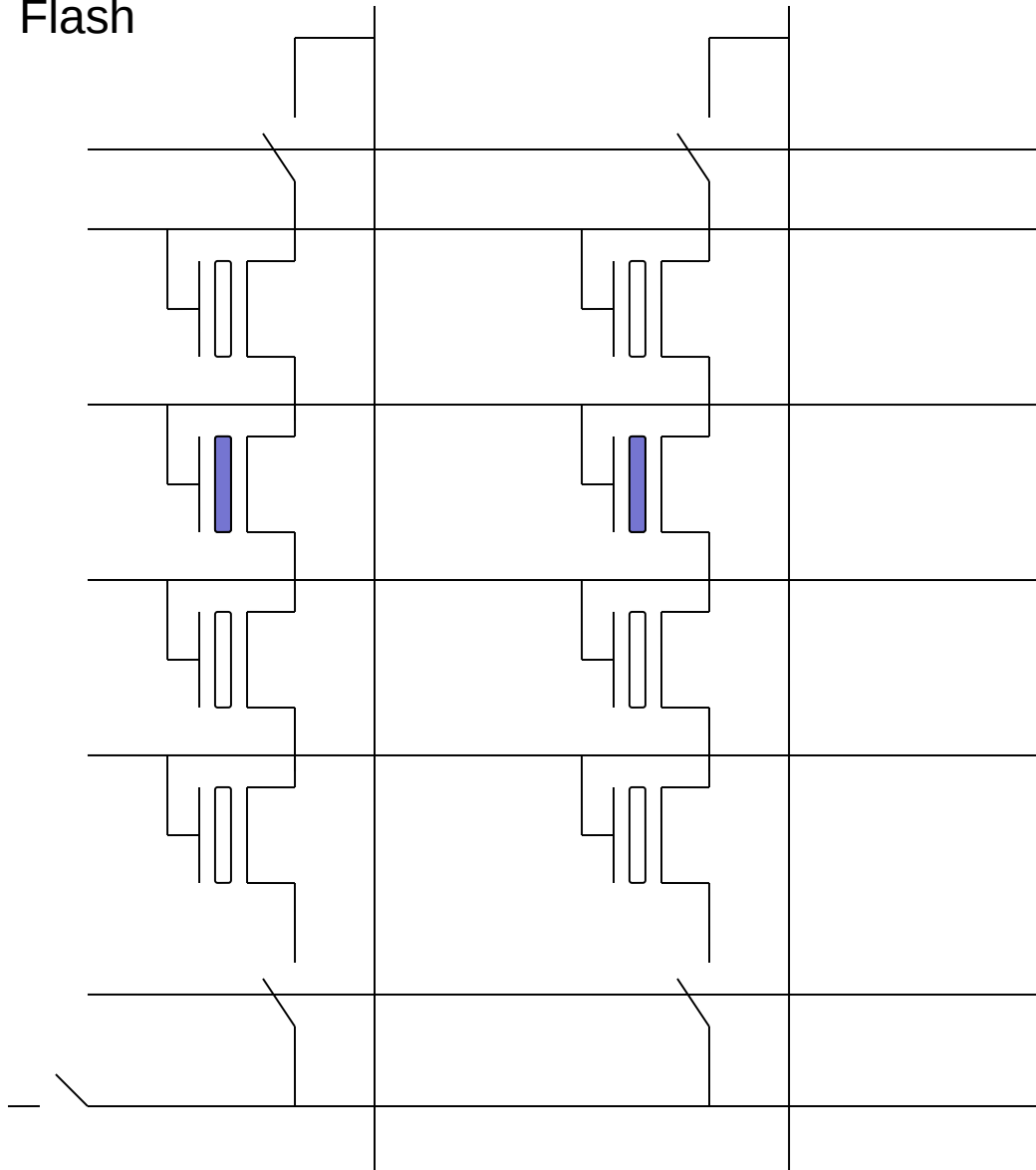
- Flash



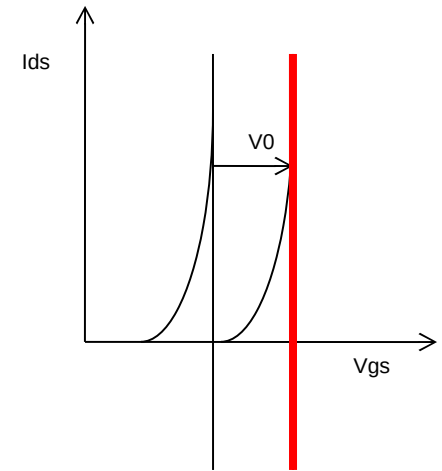
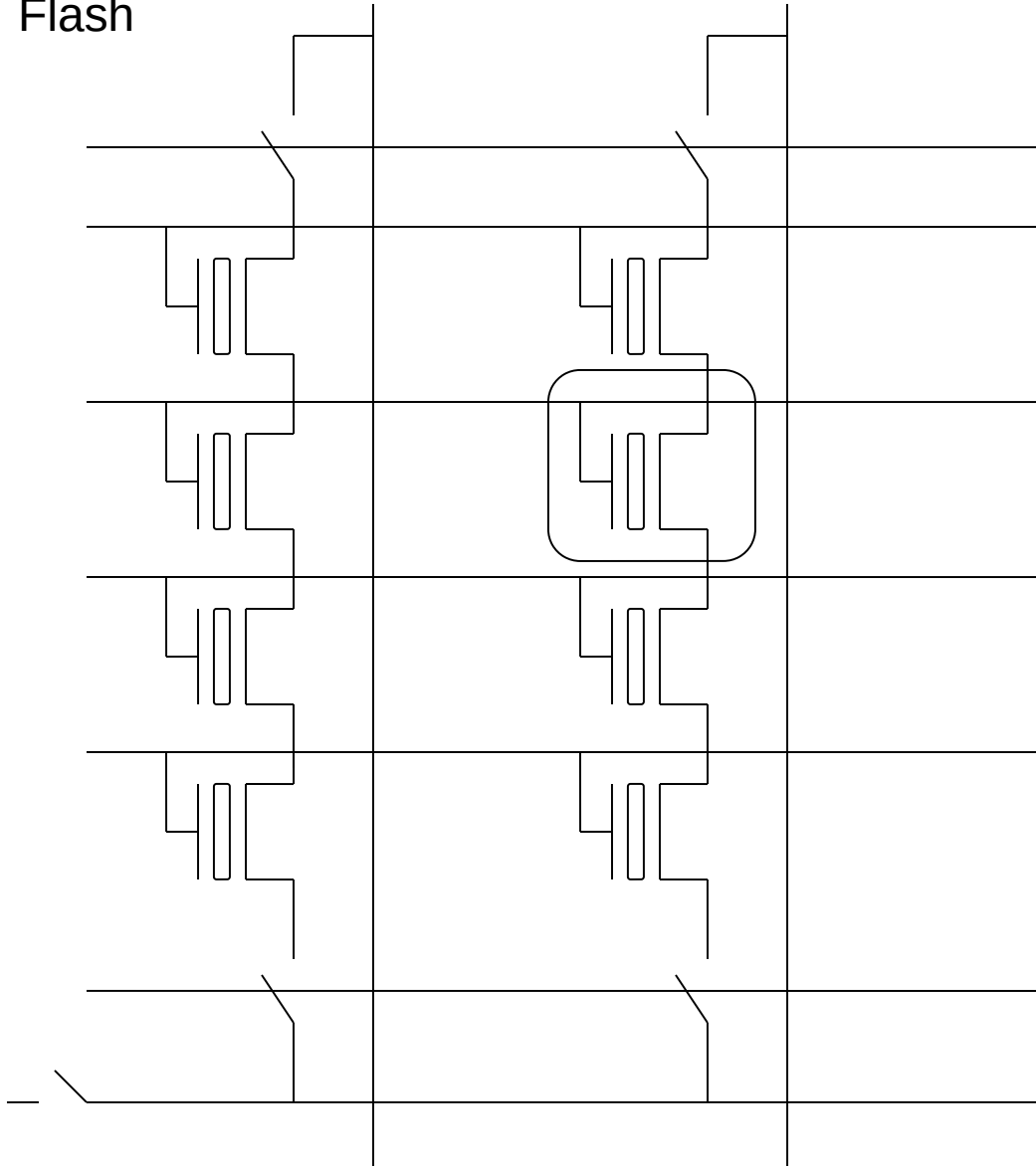
- Flash



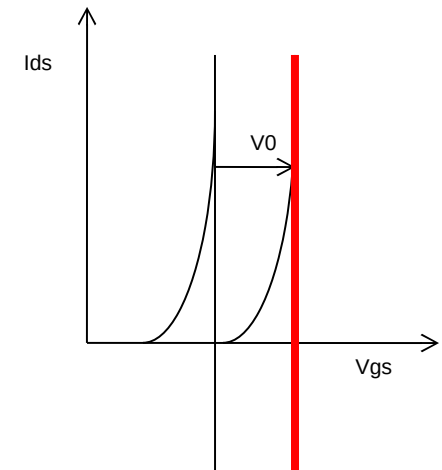
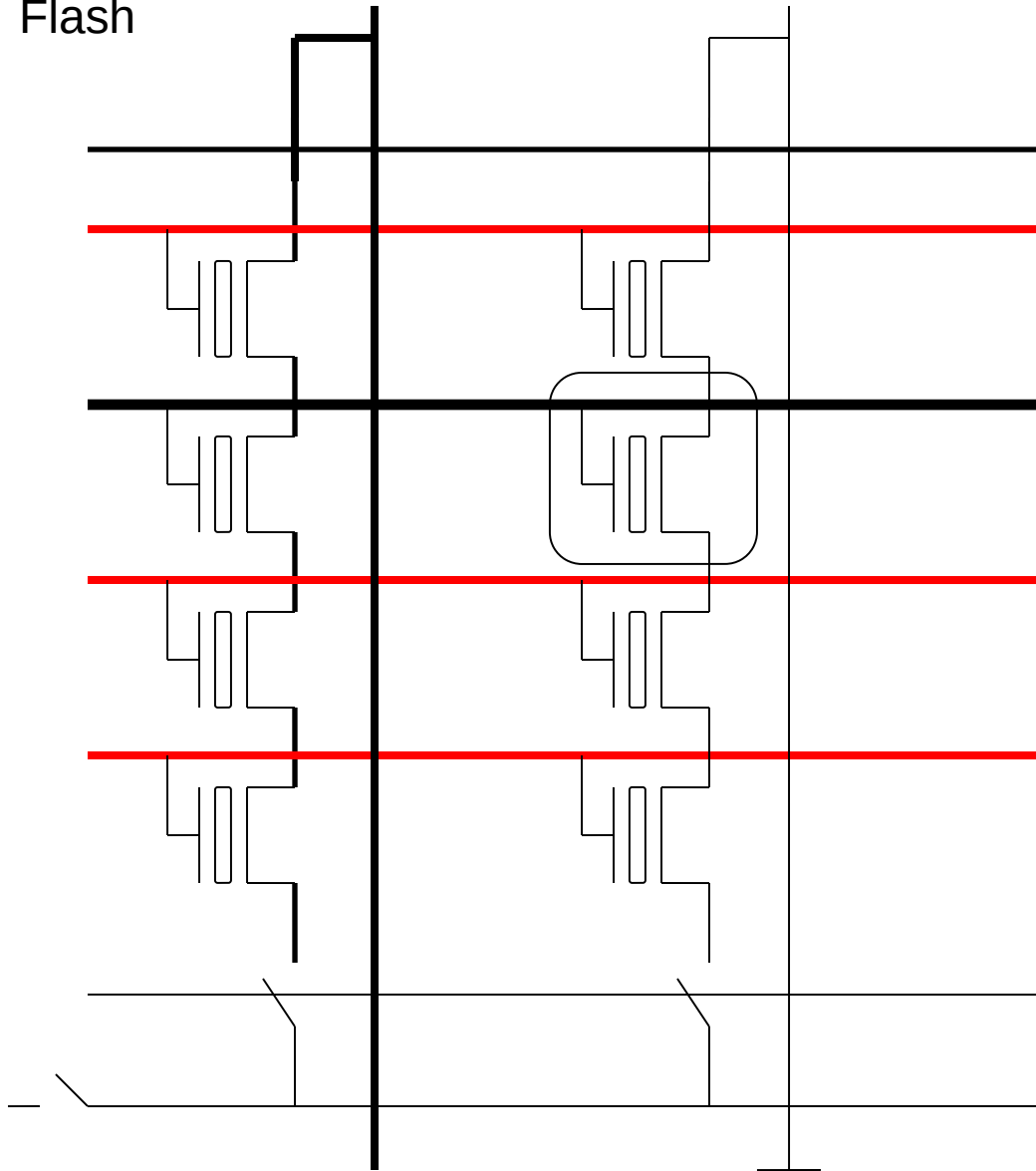
- Flash



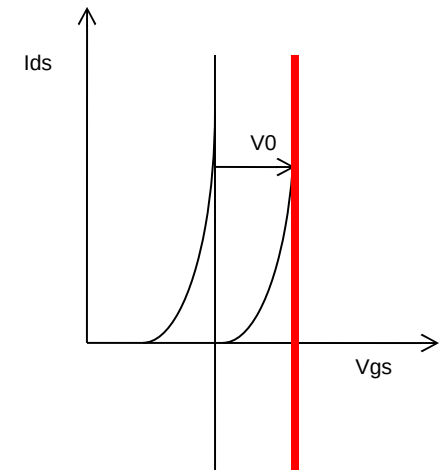
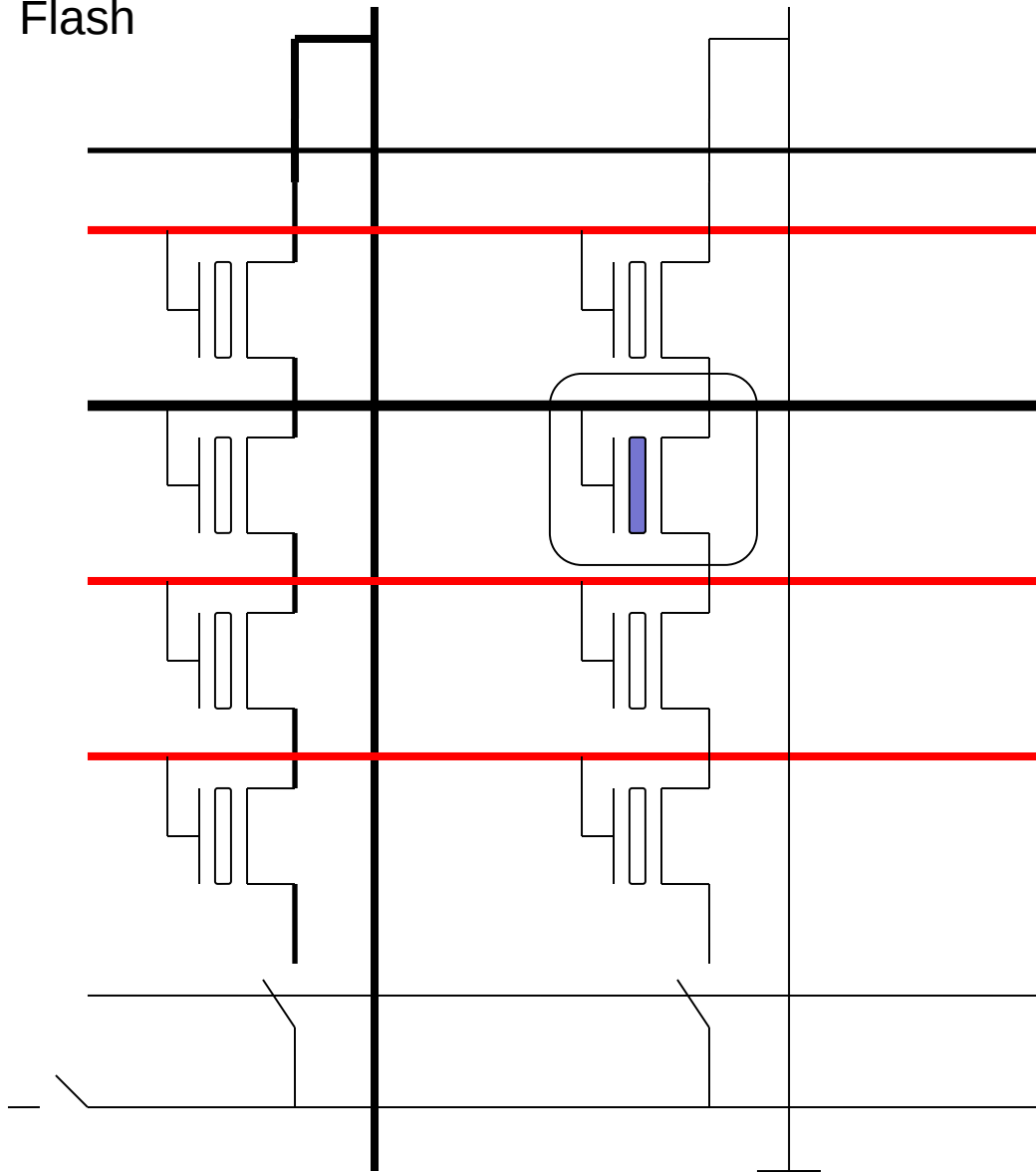
- Flash



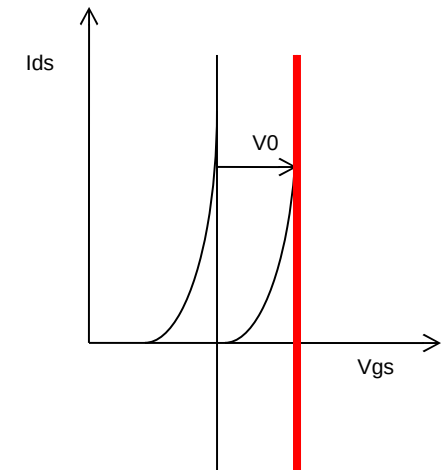
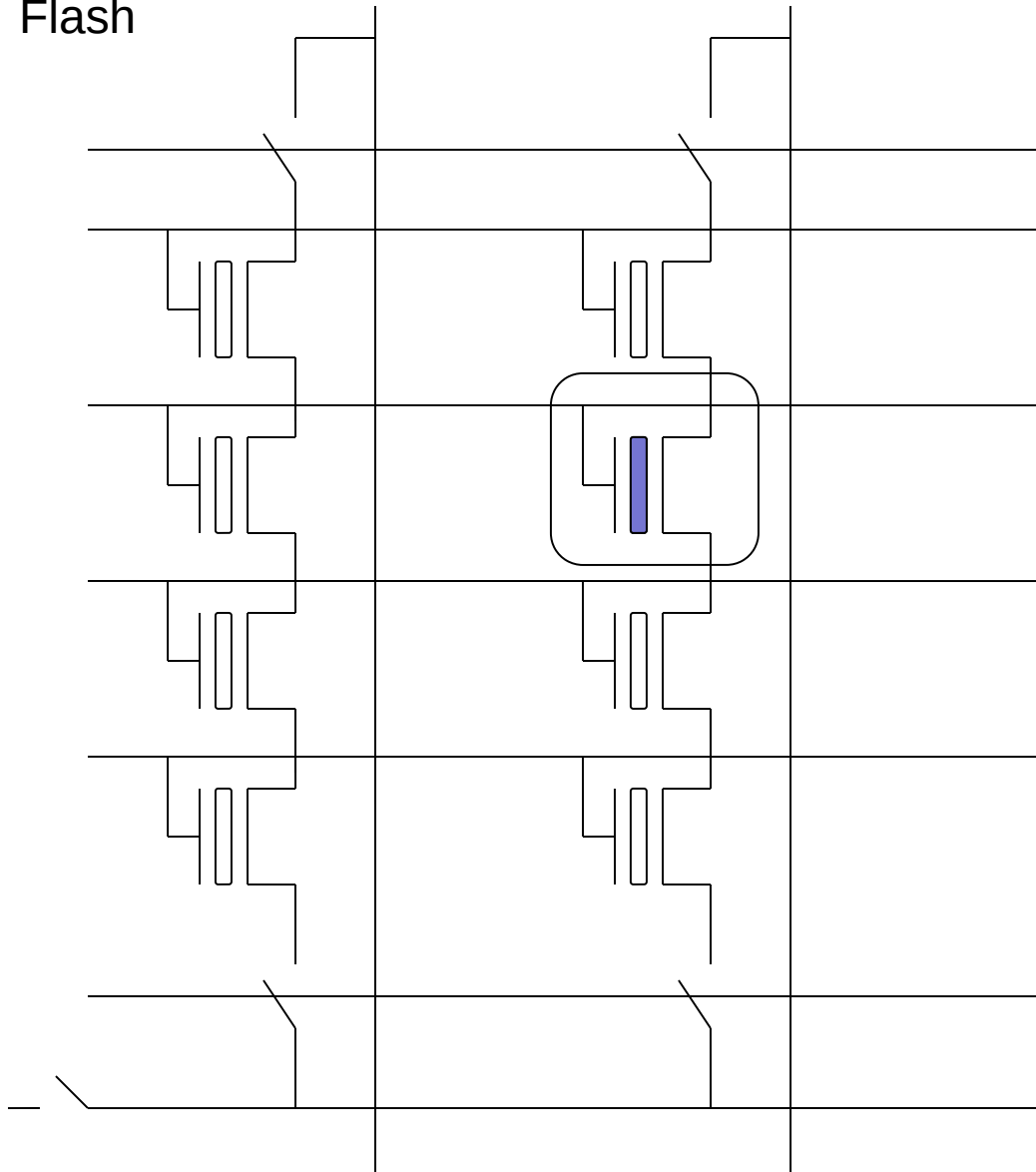
- Flash



- Flash

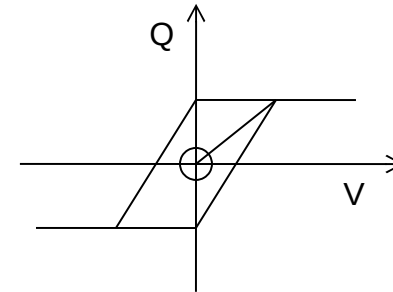
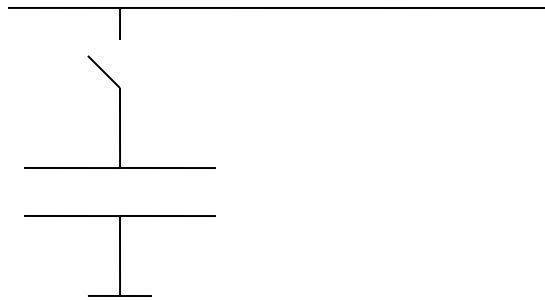


- Flash

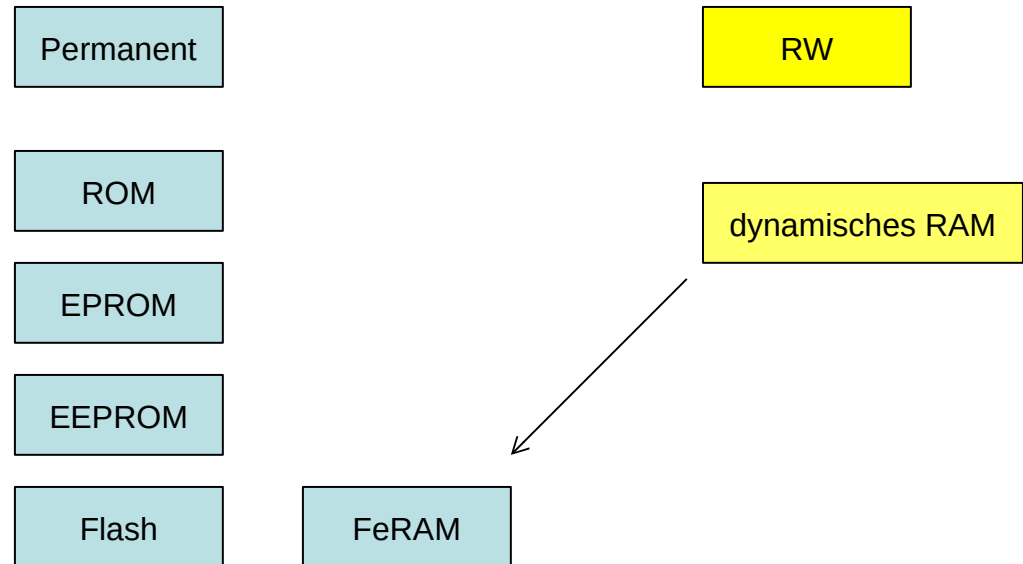


Ferroelectric RAM

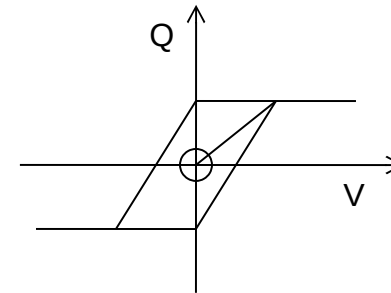
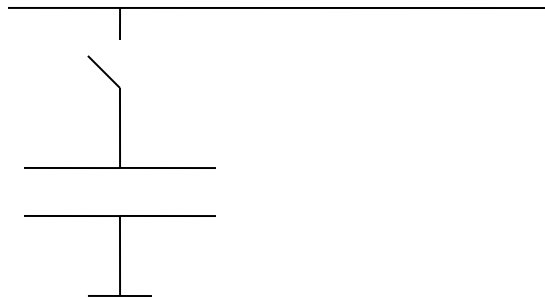
- https://en.wikipedia.org/wiki/Ferroelectric_RAM
- Struktur wie DRAM aber der Kondensator ist "permanent"
- Reading, however, is somewhat different than in DRAM. The transistor forces the cell into a particular state, say "0". If the cell already held a "0", nothing will happen in the output lines. If the cell held a "1", the re-orientation of the atoms in the film will cause a brief pulse of current in the output as they push electrons out of the metal on the "down" side. The presence of this pulse means the cell held a "1". Since this process overwrites the cell, reading FeRAM is a destructive process, and requires the cell to be re-written if it was changed.



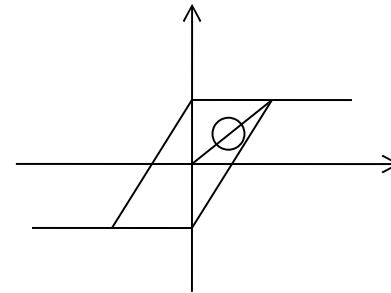
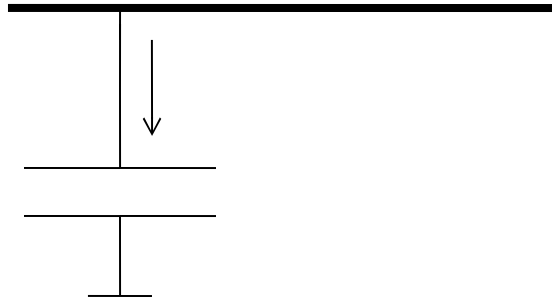
-



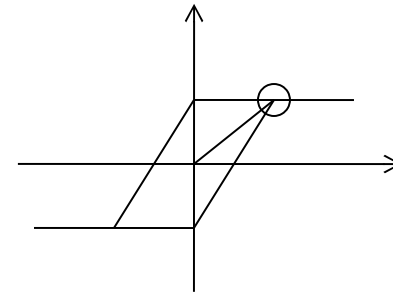
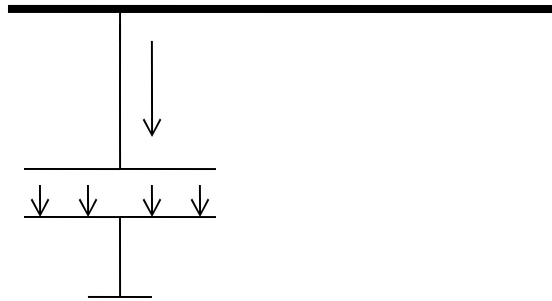
- https://en.wikipedia.org/wiki/Ferroelectric_RAM
- [Bariumtitanat](#), BaTiO_3
- Bariumtitanat ist ein [Ferroelektrikum](#) und besitzt eine ausgeprägte [Hystereseschleife](#). Wie alle Ferroelektrika besitzt es eine hohe [Permittivität](#), welche stark von der [elektrischen Feldstärke](#) abhängt



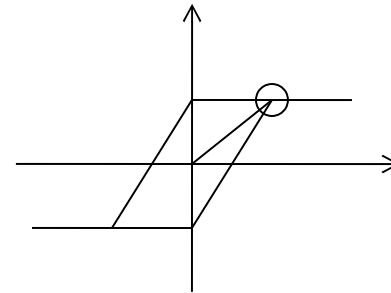
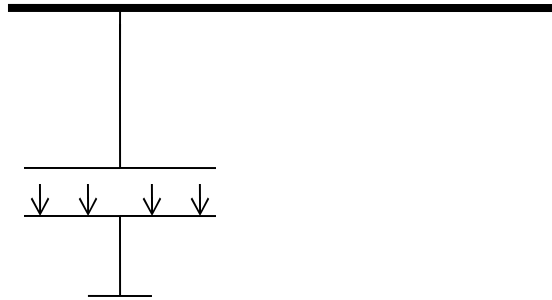
- write



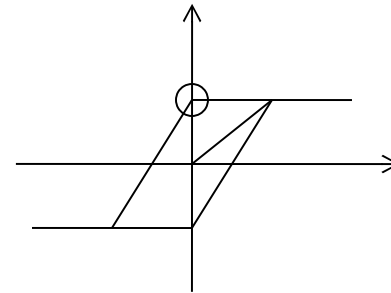
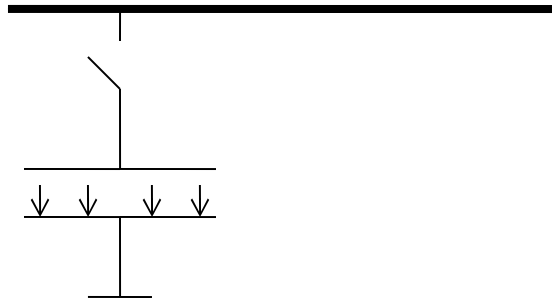
- write



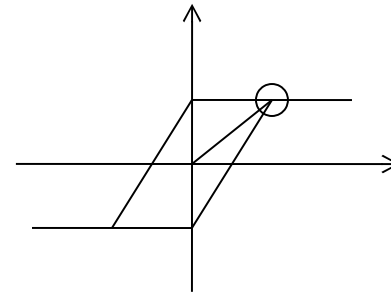
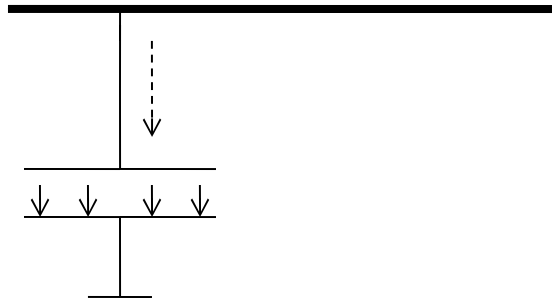
- write



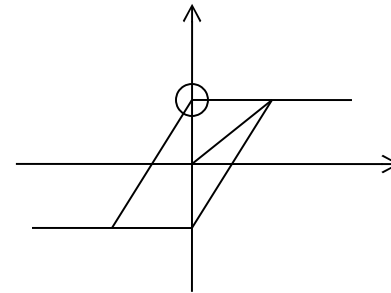
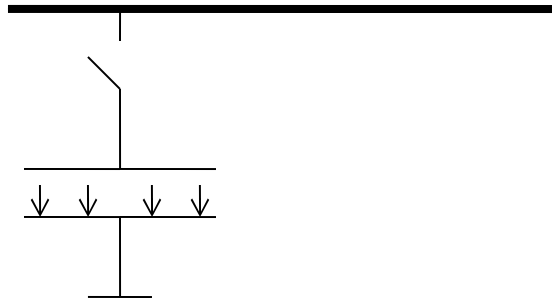
- **written**



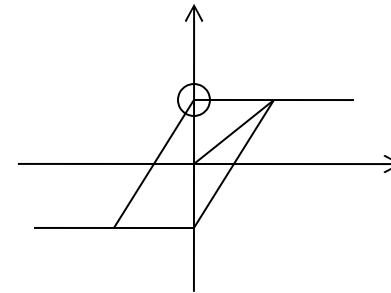
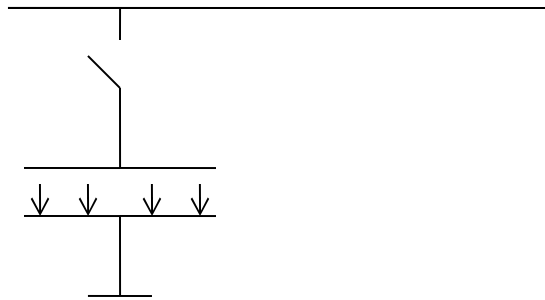
- Try read



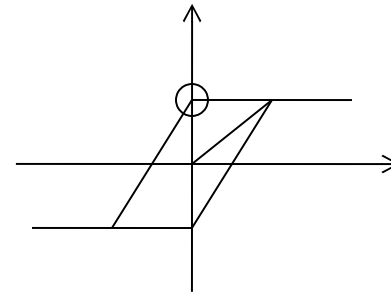
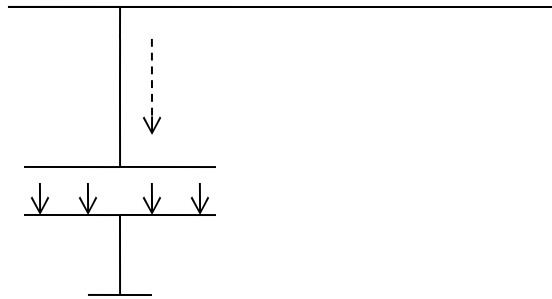
- Try read



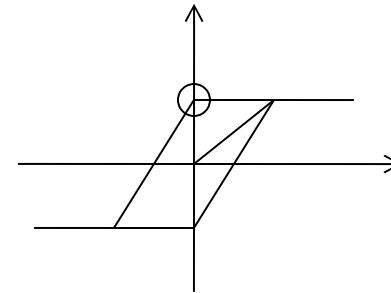
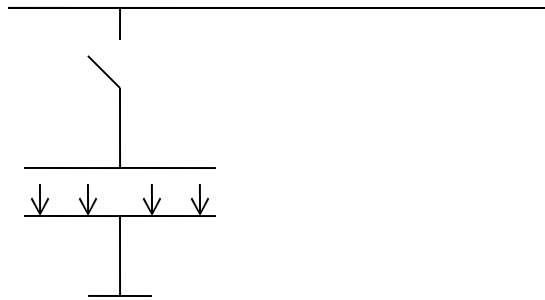
- Try read



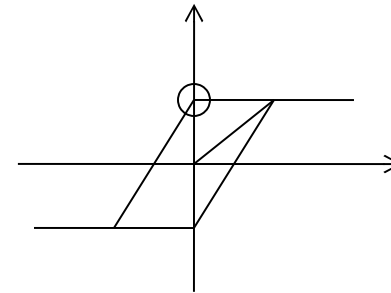
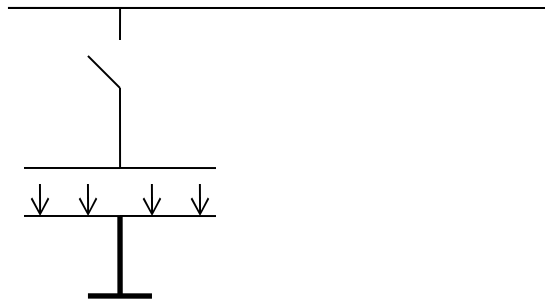
- Try read



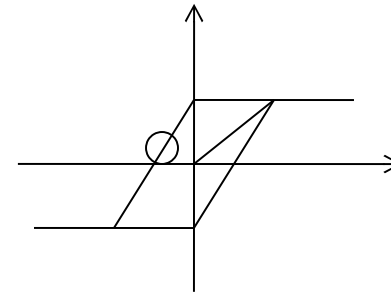
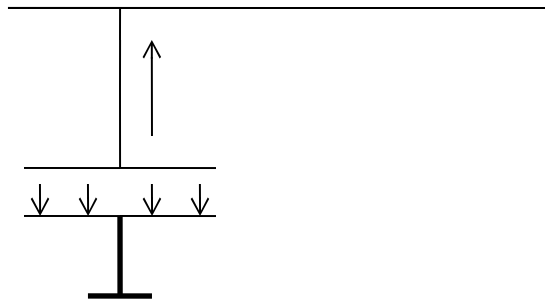
- Try read

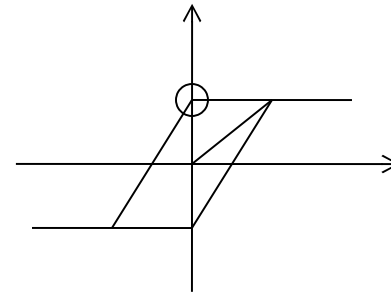
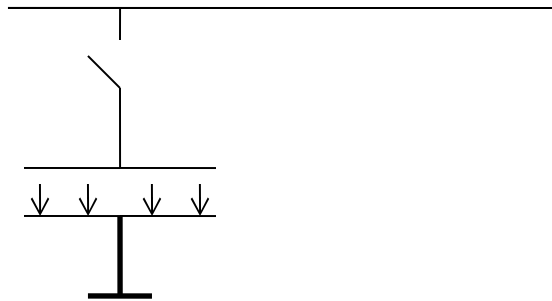


- Non destructive read

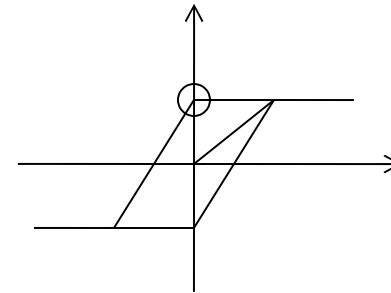
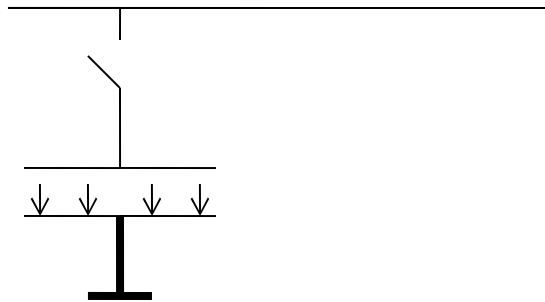


- Non destructive read

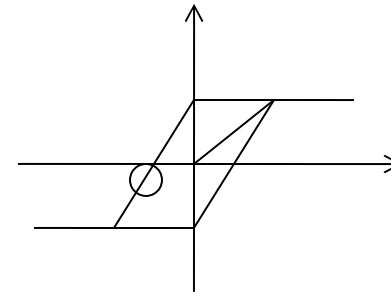
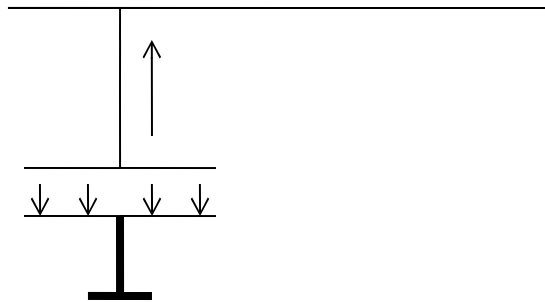




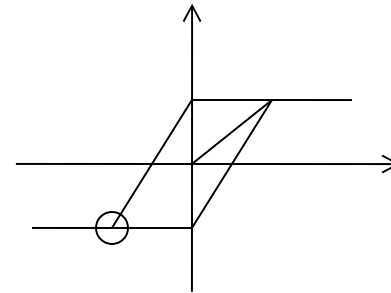
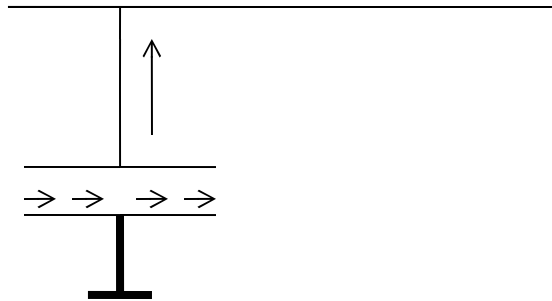
- Read with overwrite



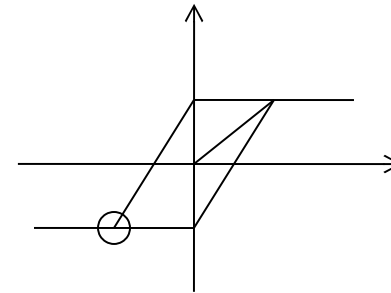
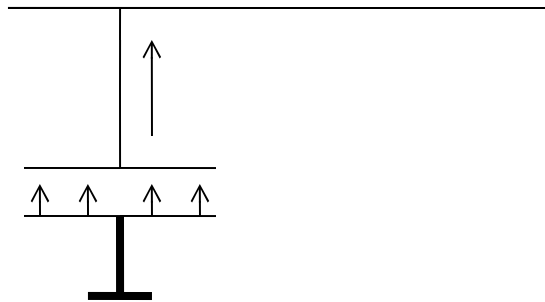
- Read with overwrite



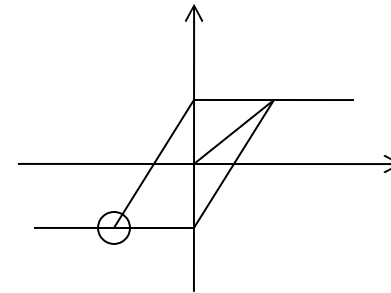
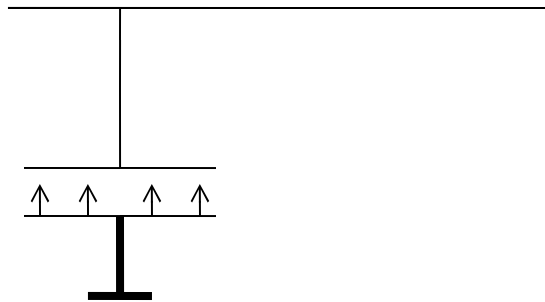
- Read with overwrite



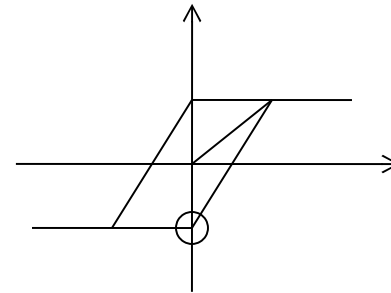
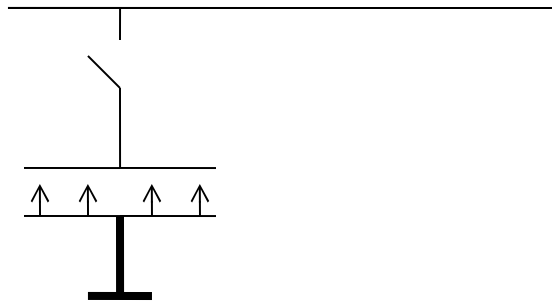
- Read with overwrite

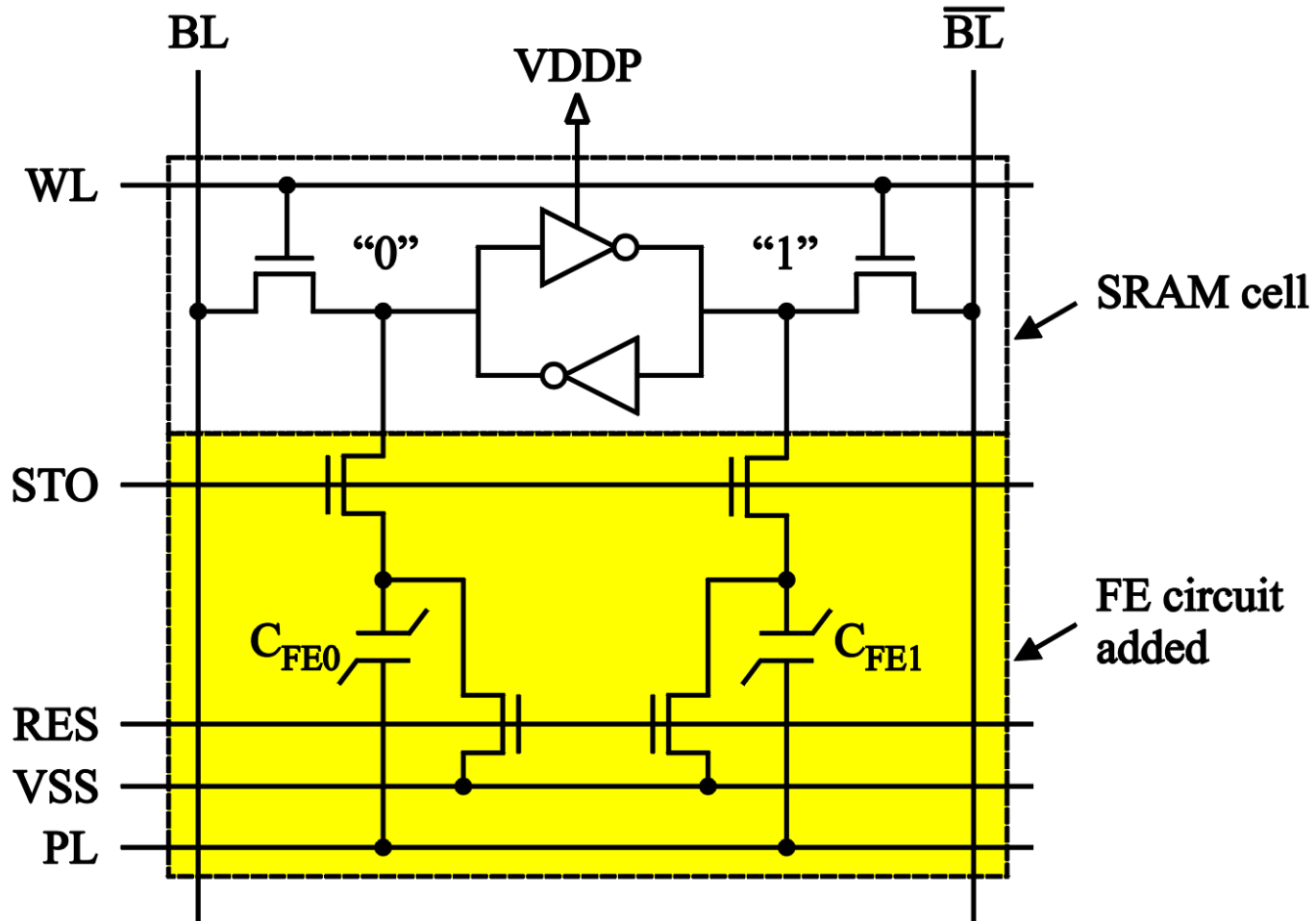


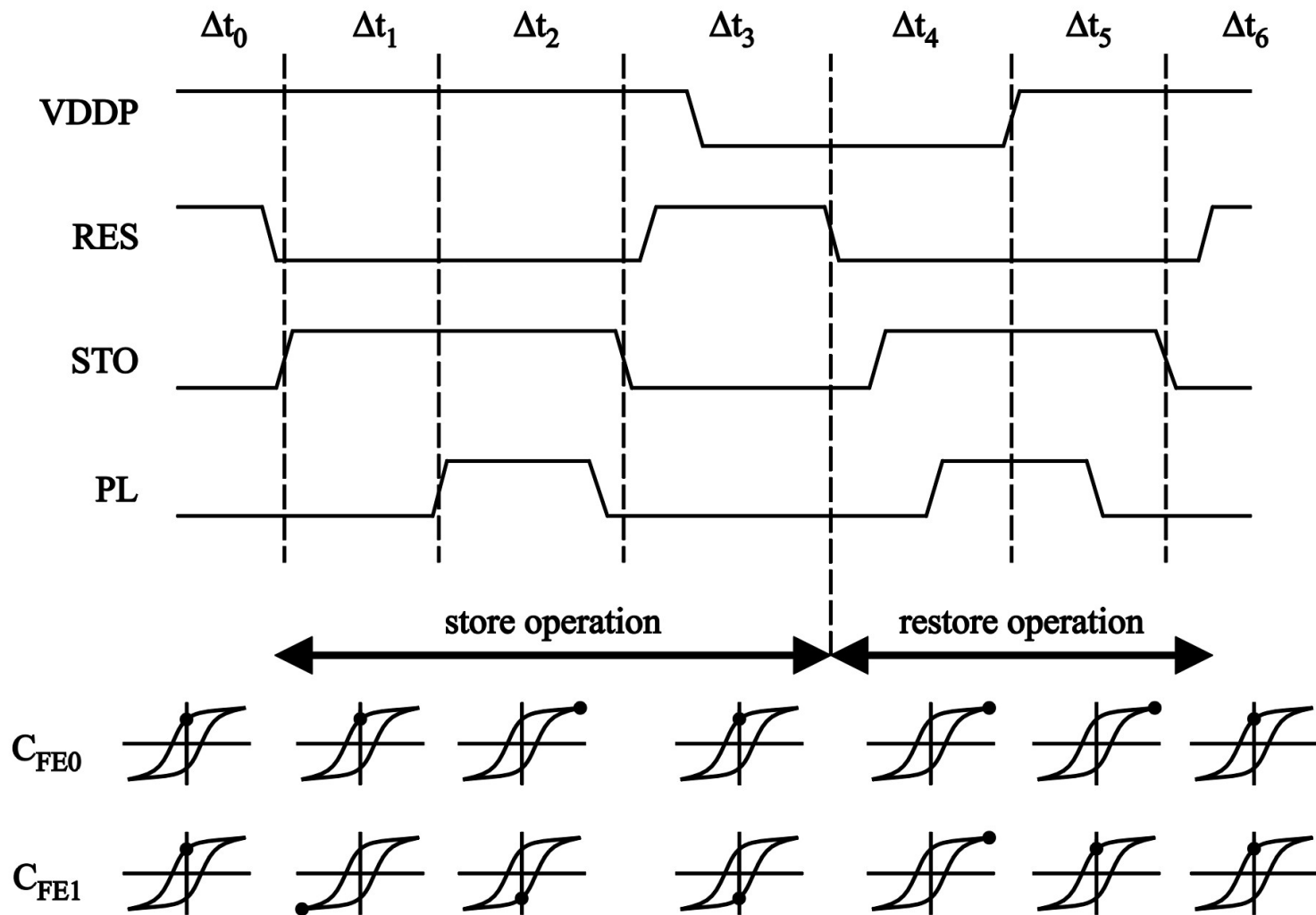
- Read with overwrite

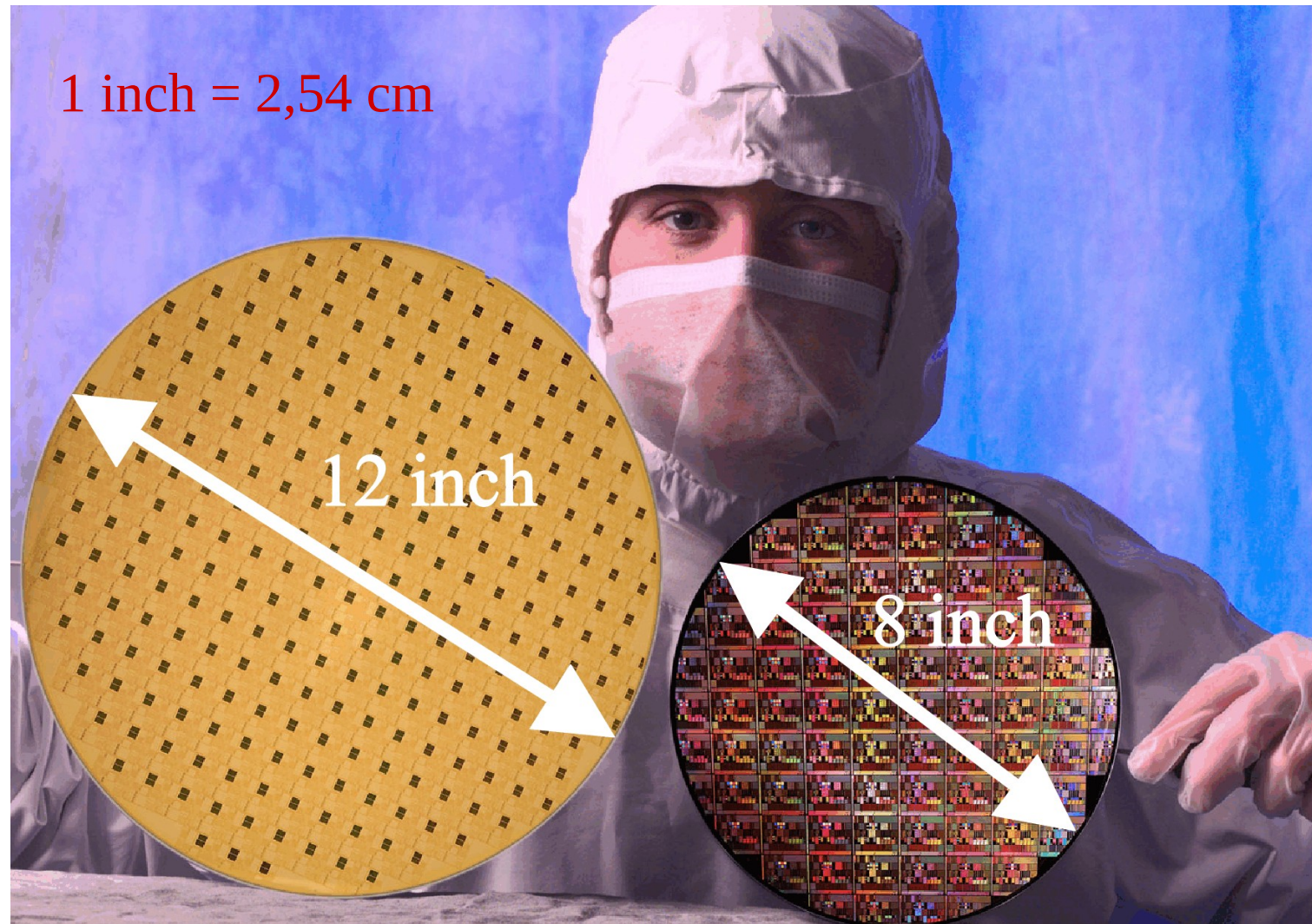


- **written**

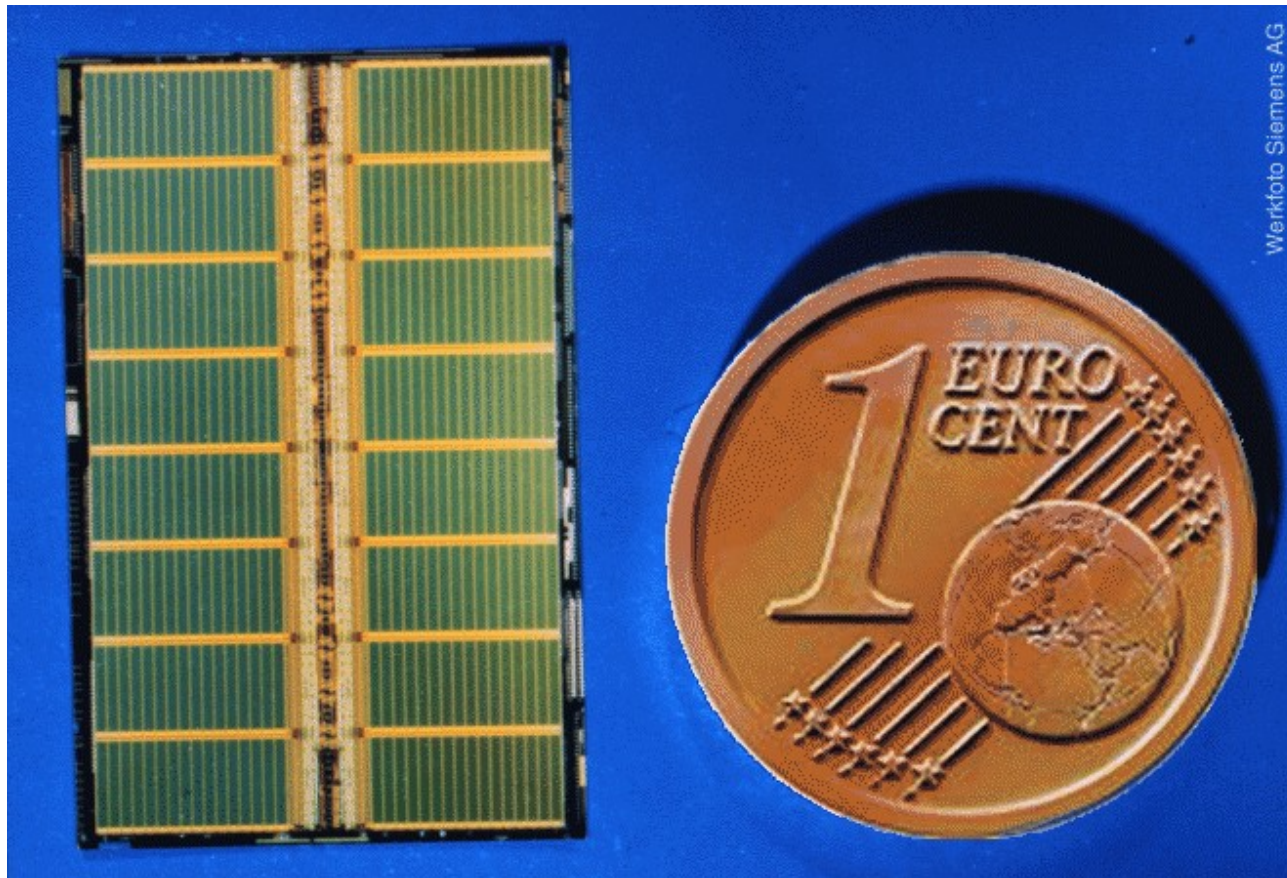








256 Mbit –Chip (16M x 16)



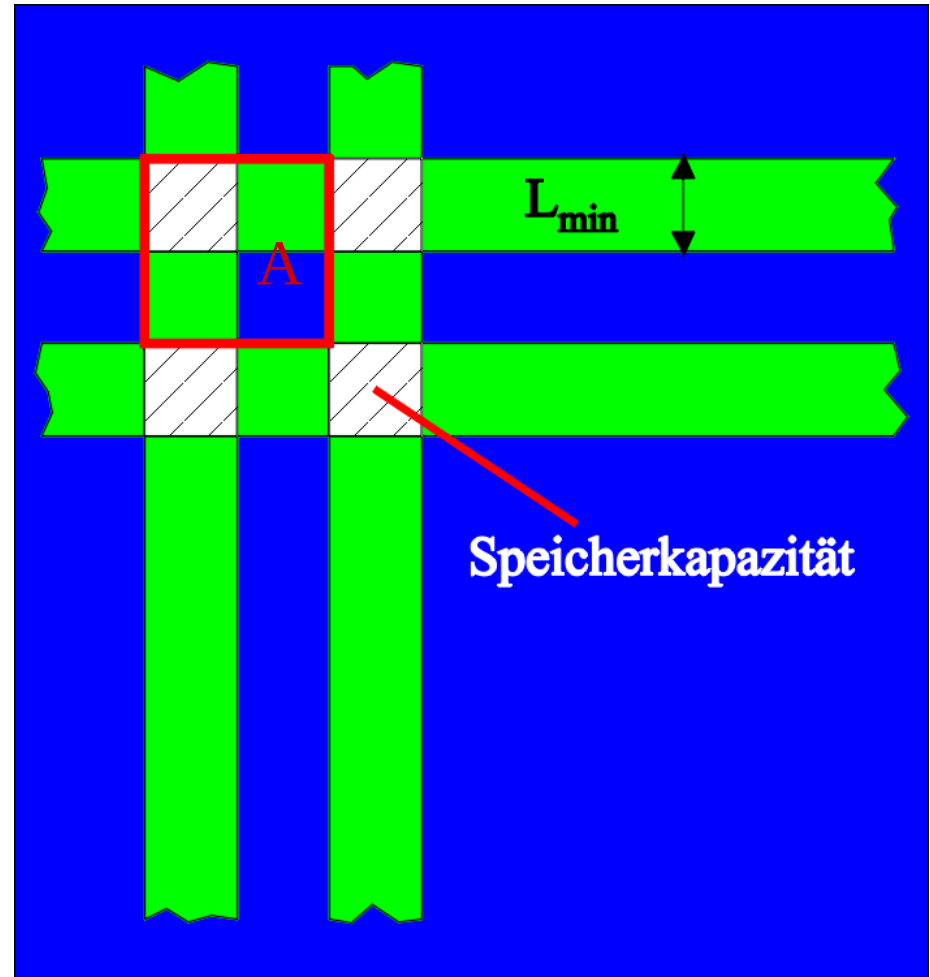
Maß für den Integrationsgrad :
Anzahl der Strukturquadrate

$$F' = \frac{A}{L_{\min}^2}$$

$$\min F' = 4$$

Häufig in der Literatur zu
finden ist die Größe F^2 :

$$F^2 = L_{\min}^2$$



FeRAM $8 - 13 F^2$

SRAM $\approx 60 F^2$

DRAM $8 F^2$

EEPROM $\approx 40 F^2$

FLASH $6 - 12 F^2$

Kleinste Strukturen auf dem Chip:

$F = L_{\min} = 45, 65, 90, 130, 180, \dots, 300 \text{ nm}$